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ELECTRONIC DESIGN

APRIL 18, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

**PREDICTABLE
TIMING ARRIVES
FOR SUBMICRON
ASIC DESIGN**

**TECHNOLOGY ANALYSIS:
1.8-IN. HARD-DISK
DRIVES**

**IMPROVING THE
DIALOGUE BETWEEN
ENGINEERING AND
MARKETING**

**COMPUTERS/
EMBEDDED SYSTEMS
DESIGN SECTION**

PEASE PORRIDGE



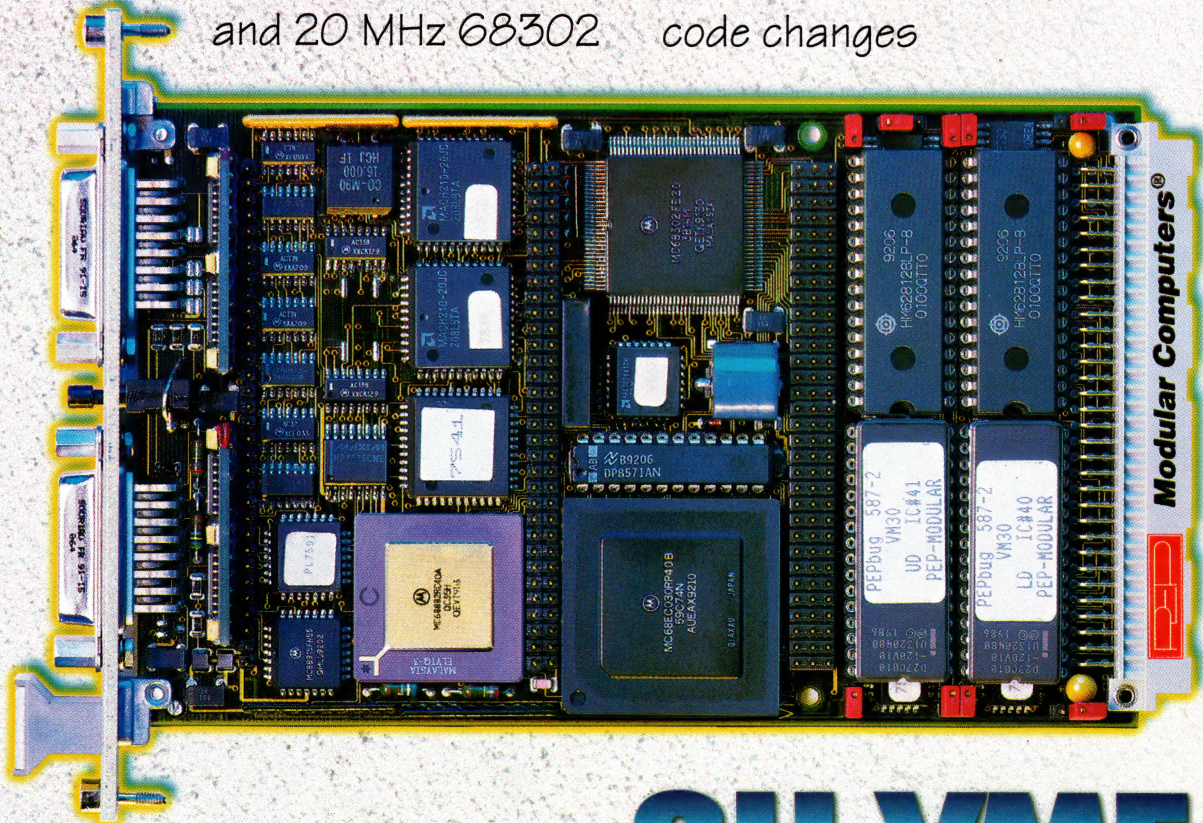
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QuickLook

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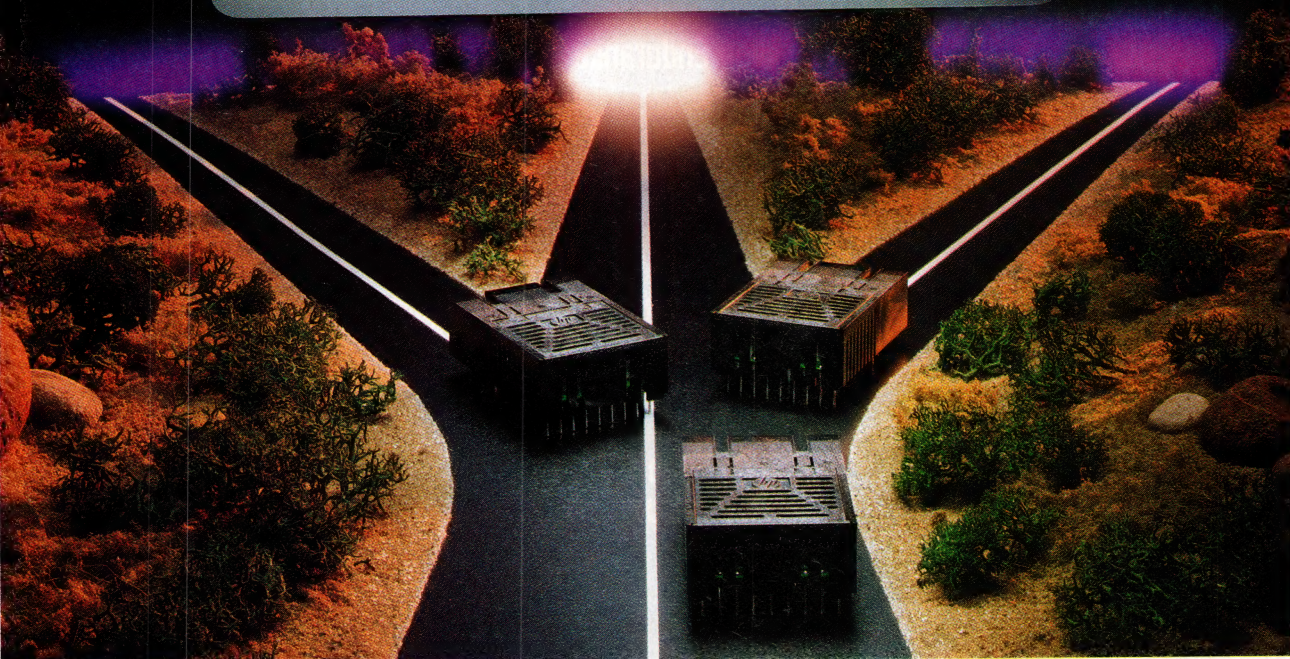
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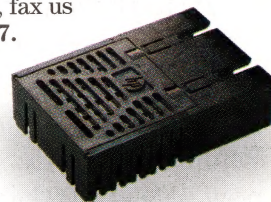
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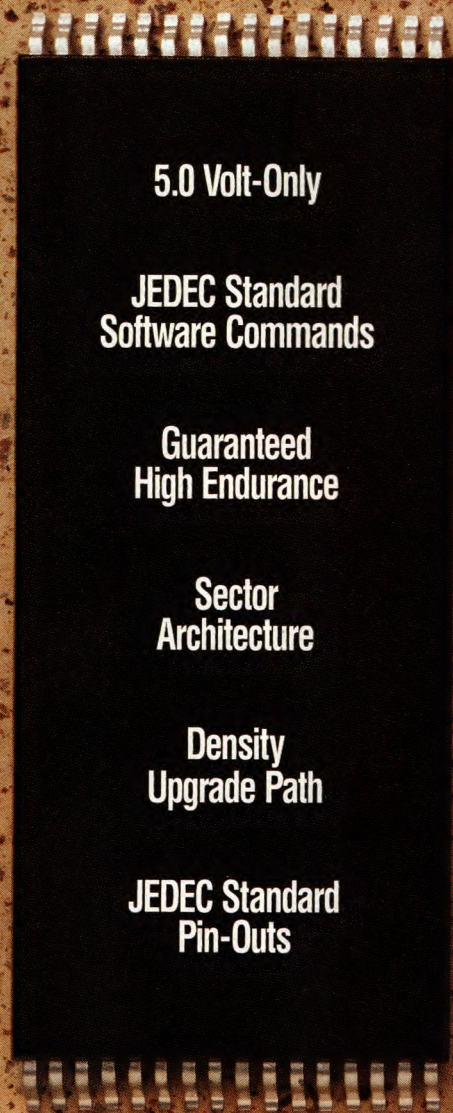


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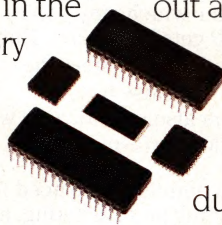
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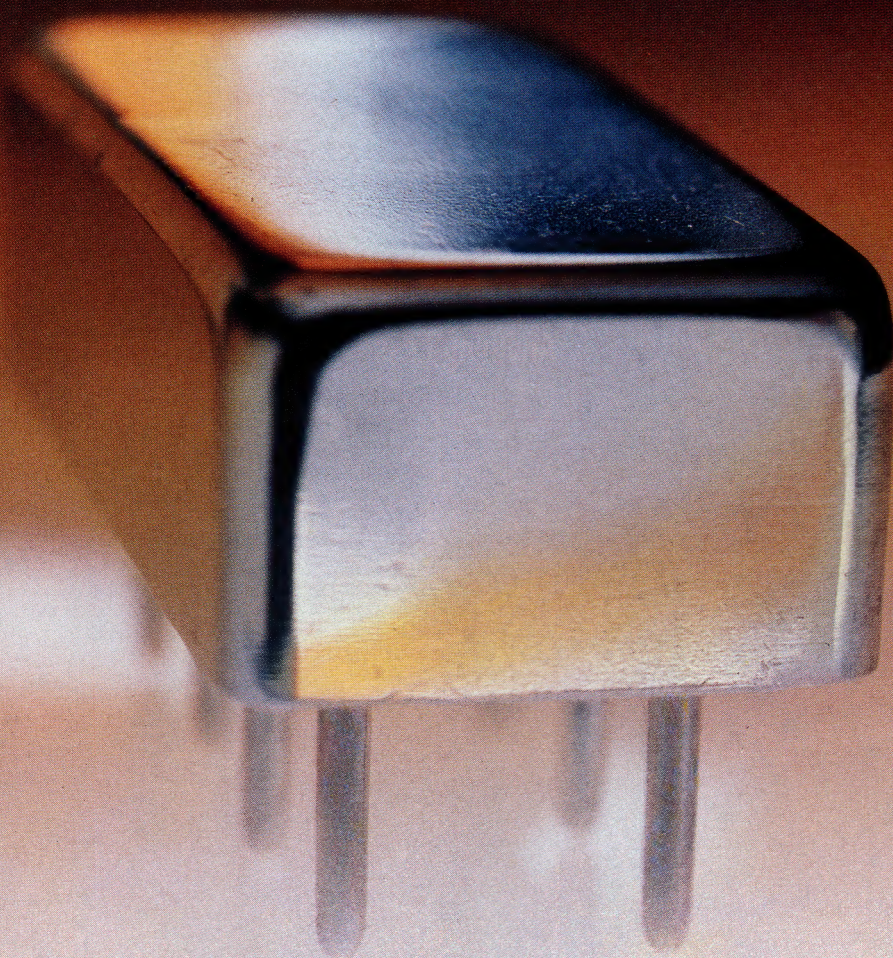
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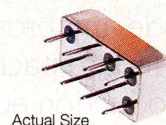
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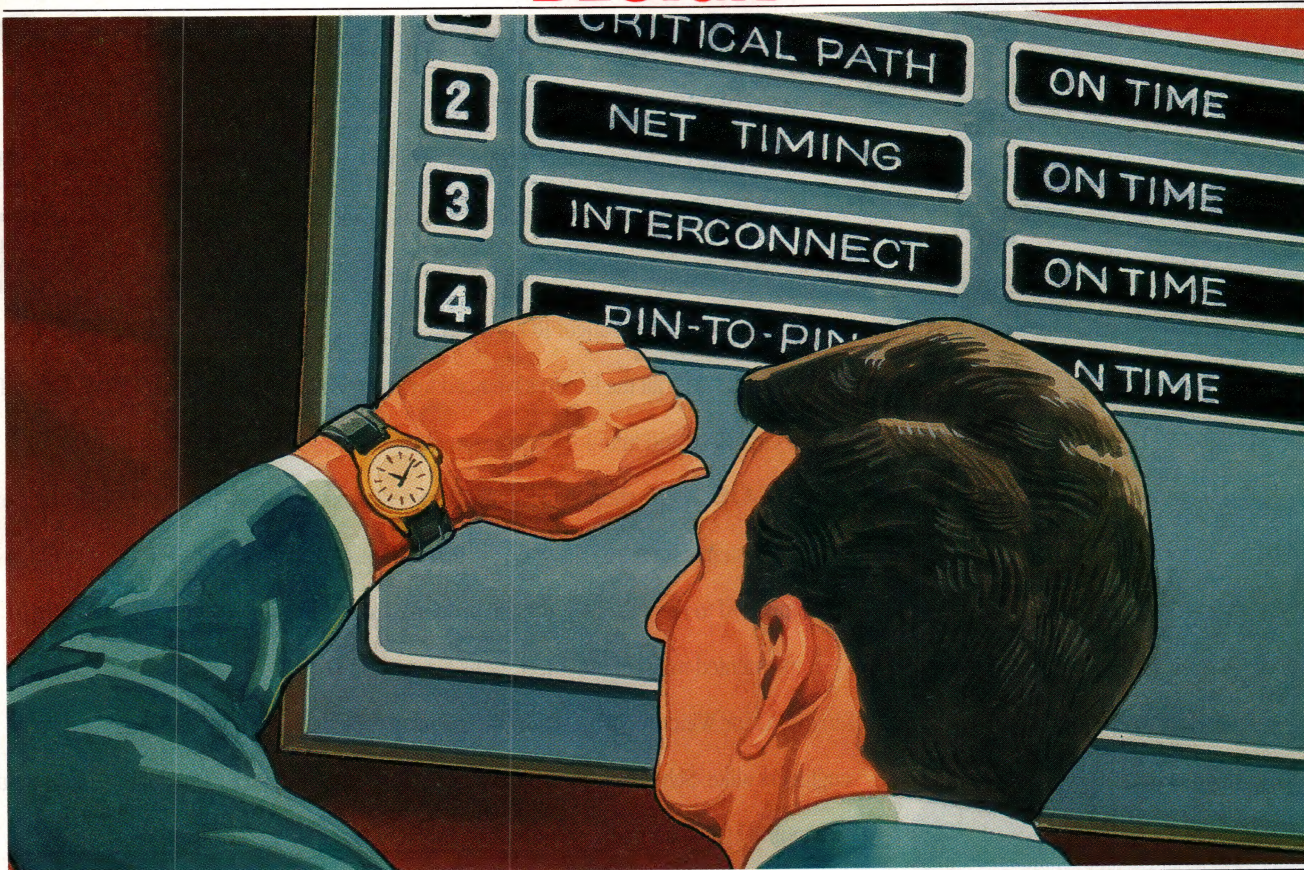
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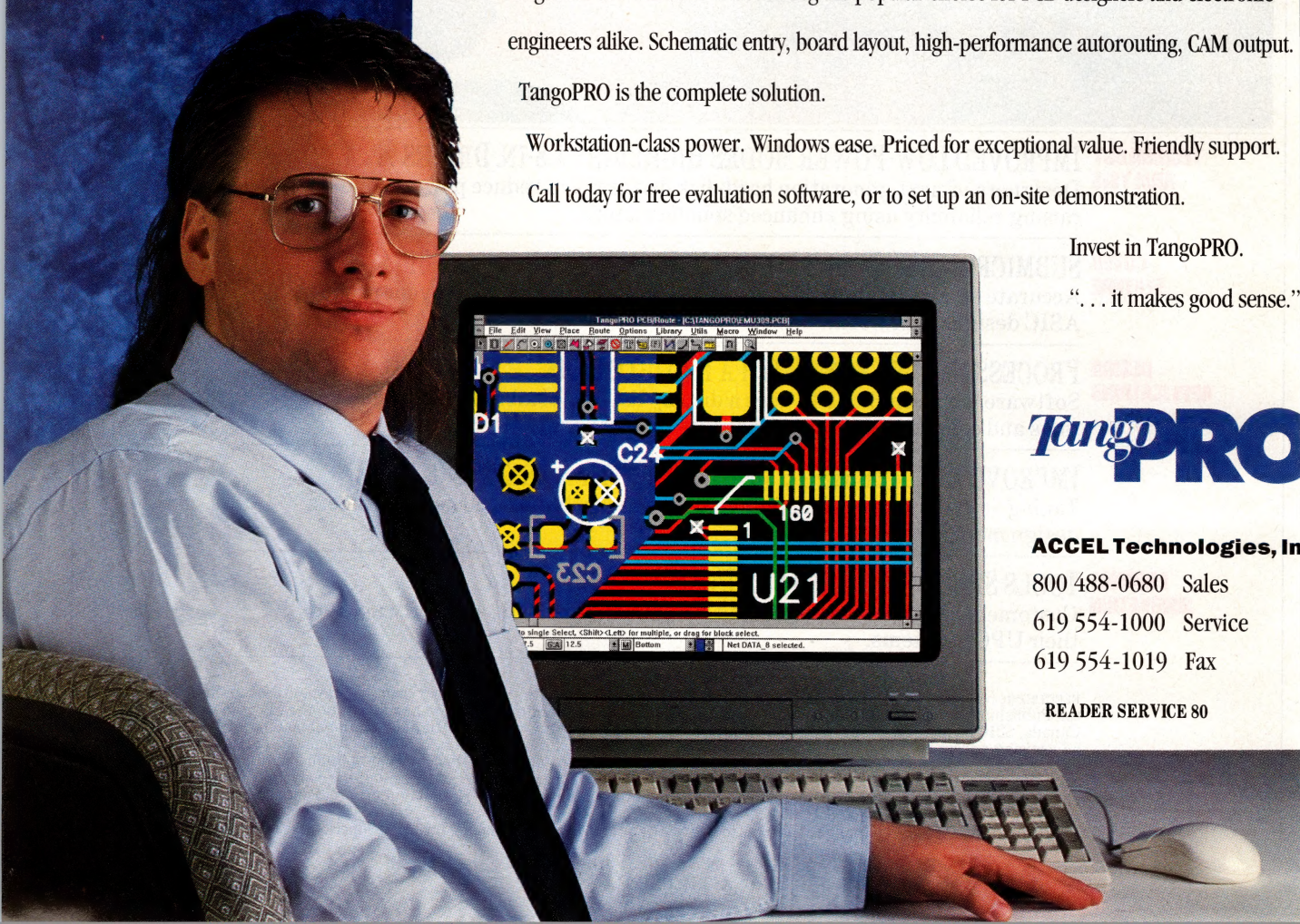
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1967 First Place Award
1968 First Place Award
1972 Certificate of Merit
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40
YEARS AGO

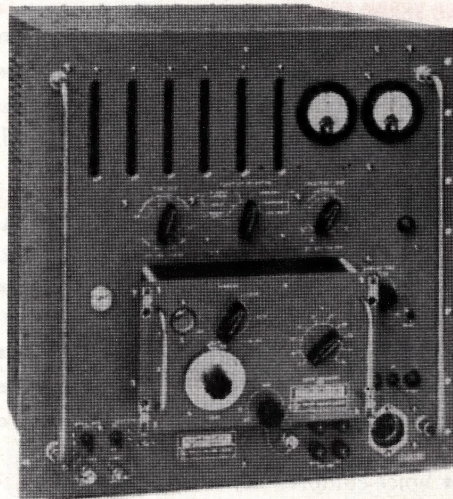
Electronic counter: Direct reading, accurate unit

With this direct-reading Model 524B Electronic Counter, one can measure transmitter and crystal oscillator frequencies; electronic, electrical, and mechanical time intervals; pulse lengths and repetition rates; frequency drift; and make high accuracy ballistics time measurements or high resolution tachometry measurements. The instrument is also a precision frequency standard with an accuracy of $1/1,000,000 \pm 1$ count. The unit employs four plug-in units which extend range, increase sensitivity, or provide time interval measuring circuits.

The basic range of the instrument itself is 10cy to 10Mc for frequency counting, or zero cycles to 10kc for period measurements. Cabinet size is 19" wide x 19-1/4" x 17" deep, and the instrument weighs 112 lb. Hewlett-Packard Company, 395

Page Mill Road, Palo Alto, Calif. (*Electronic Design*, April 1954, p. 72.)

Today, HP offers a 100-MHz counter, the HP 5314A, for \$850 in a cabinet measuring 9 3/8 by 3 7/8 by 10 7/8 in. and weighing 4.4 lb.—SS



Low torque 'Helipot's' combine small size, high precision

An improved version of the series "T" miniature "Helipot's" features low torque, small size, and precision. All-metal housing and lids provide dimensional stability, ruggedness, and maximum heat dissipation. Maximum operating temperature has been raised to 105°C ambient. Power rating has been increased to 1.2w at 40°C ambient. While standard linearity tolerance remains $\pm 0.5\%$, best practical linearity tolerance is now $\pm 0.2\%$. Standard electrical rotation has been increased to 354°. Resistance range is as low as 10 ohms and as high as 100,000 ohms. Helipot Corp., 916 Meridian Ave., South Pasadena, Calif. (*Electronic Design*, April 1954, p. 60.)

In addition to these high-quality helical potentiometers, Helipot made another "contribution" to the industry: a series of poster-size cartoons that proliferated throughout design labs. My favorite one showed a vacant-eyed, smiling young man with an apple on his head and an arrow in his forehead. The caption read "Have faith. Keep smiling." (Or something close to that.)—SS

New Books: Modulation Theory ... By Harold S. Black, 363 pages. D. Van Nostrand Company, Inc. 250 Fourth Ave., New York 3, NY \$8.75.

Written for advanced students and practicing engineers, this book covers the fundamentals of modulation theory in the light of recent progress in this and related fields. Communication engineers are now able to use the advances in communication theory to realize more efficient system design by taking into account the statistical structure of the original message and the matching of the information signals to the noisy channel. The book stems from material used in the Communication Development training program of the Bell Telephone Laboratories. The first eight chapters cover the general philosophy of the subject: Topics include historical background, reasons for modulating, the sampling principle, quantizing, code transmission, multiplexing, speed of signaling and channel capacity; and reduction of signal power through the use of redundant codes. The last twelve chapters contain theoretical treatments of various modulation systems. (*Electronic Design*, April 1954, p. 88.)

Bell Labs' Harold S. Black is best known for his invention of the negative-feedback amplifier.—SS



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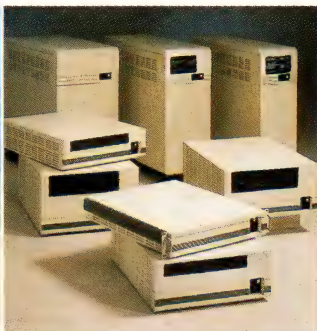
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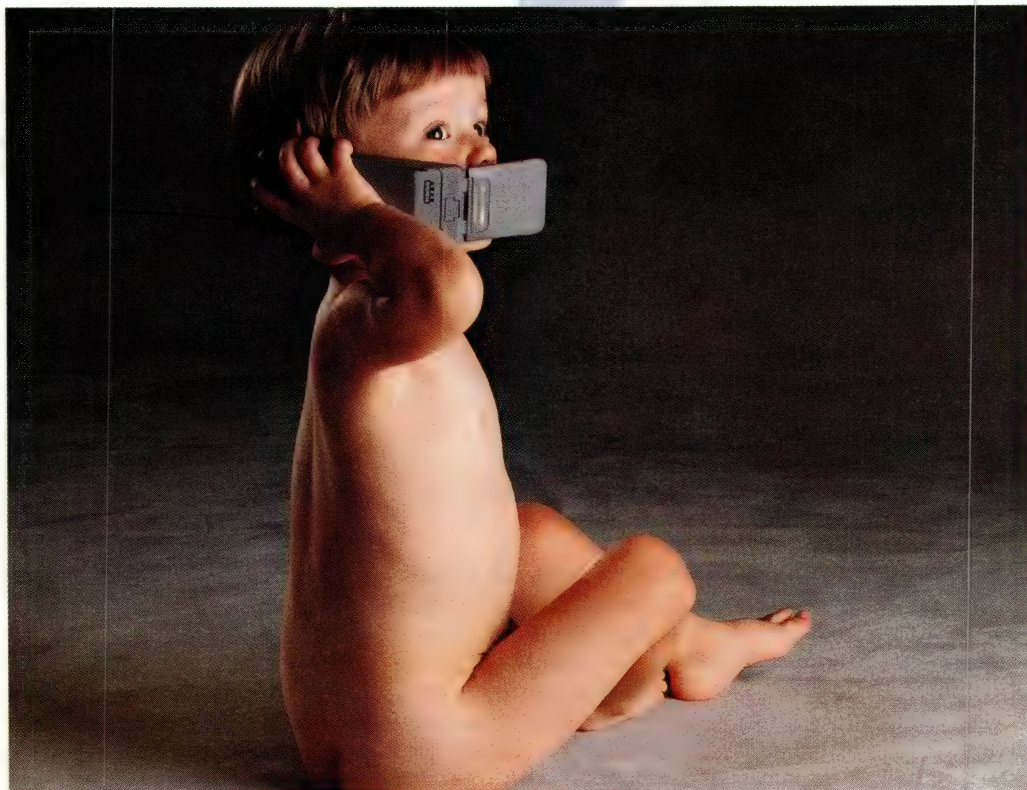
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UPCOMING MEETINGS

APRIL

1994 IEEE 44th Electronic Components and Technology Conference (ECTC '94), Apr. 30-May 5. Washington Hilton Hotel, Washington D.C. Contact James Bruorton, Kemet Electronics, P.O. Box 5928, Greenville, SC 29606; (803) 963-6621; fax (803) 963-6521.

MAY

1994 IEEE Custom Integrated Circuits Conference (CICC '94), May 1-4. Town & Country Hotel, San Diego, CA. Contact Melissa Widerkehr, Widerkehr and Assoc., 1545 18th St. NW, Washington D.C. 20036; (202) 986-2166; fax (202) 986-1139.

VHDL International Users' Forum (VIUF), May 1-4. Co-located with the CFI 1994 Conference, Claremont Resort & Spa, Oakland, CA. Contact Ronald Waxman, University of Virginia, Dept. of EE, Thornton Hall, Charlottesville, VA 22903-2442; (804) 924-6986; fax (804) 924-8818; E-mail: Ronw@virginia.edu.

ICC/Supercomm '94 - 1994 International Conference on Communications, May 1-5. Ernest N. Morial Convention Center, New Orleans, LA. Contact Eddie Sawaya, So. Central Bell Telephone, 365 Canal St., Room 710, New Orleans, LA 70140; (504) 528-2673; fax (504) 528-7170.

Networld + Interop 94, May 2-6. Las Vegas Convention Center, Las Vegas, NV. Contact Nancy Garafano, Ziff-Davis Exposition and Conference Co., 303 Vintage Park Dr., Foster City, CA 94404-1138; (415) 578-6900; fax (415) 525-0194.

1994 Electronic CAD Interoperability and Integration Conference (EII'94), May 4-6. Claremont Hotel, Oakland, CA. Contact Don Cottrell, program chair, CAD Framework Initiative Inc., 4030 W. Braker Ln., Suite 550, Austin, TX 78759; (512) 338-3379; E-mail: Contrell@cfi.org.

1994 IEEE International Conference on Robotics and Automation, May 8-13. San Diego Princess Resort, San Diego, CA. Contact Harry Hayman, Box 3216, Silver Spring, MD 20918; (301) 236-5621; fax (301)

236-5621.

1994 Conference on Lasers & Electro-Optics/The International Electronics Conference (CLEO/IQEC), May 8-13. The Anaheim Convention Center, Anaheim, CA. Contact IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; phone (908) 562-3893; fax (908) 562-1571.

ELECTRO 94, May 10-12. Hynes Convention Center, Boston, MA. Contact Ms. Sharon Schifano, Miller Freeman Inc., 13760 Noel Rd., Suite 500, Dallas, TX 75240; (800) 527-0207; fax (214) 419-7915.

1994 IEEE Instrumentation & Measurement Technology Conference - IMTC '94, May 10-12. Grand Hotel Hamamatsu, Hamamatsu, Japan. Contact Mr. Robert Myers, Myers-Smith Inc., 3685 Motor Ave., Suite 240, Los Angeles, CA 90034-5750; (310) 287-1463; fax (310) 287-1851.

1994 IEEE International Conference on Computer Languages (ICCL '94), May 16-19. Universite Paul Sabatier, Toulouse, France. Contact IEEE Computer Society, Conference Dept., 1730 Massachusetts Ave. NW, Washington, D.C. 20036-1992; (202) 371-1013; fax (202) 728-0884.

7th Annual International Software Quality Week Conference - May 17-20. Sheraton Palace Hotel, San Francisco, CA. Contact Rita M. Bral, 625 Third St., San Francisco, CA 94107-1997; (415) 957-1441; fax (415) 957-0730.

ICA Expo Dallas '94, International Communications Association, May 22-26. Dallas Convention Center, Dallas, TX. Contact Banner & Greif Ltd., 370 Lexington Ave., New York, NY 10017-6589; (212) 687-7730; fax (212) 949-9806.

The 6th International Symposium on Power Semiconductor Devices & ICs (ISPSD '94), May 31-June 2. Congress Center Davos, Davos, Switzerland. Contact ISPSD '94, Integrated Systems Laboratory, ETH

Zentrum, ETZ, CH-8092 Zurich-Switzerland; phone +41 1 632 42 68; fax +41 1 252 09 94.

JUNE

Applied Machine Vision '94, June 6-9. Sheraton Park Place, Minneapolis, MN. Contact Lisa Moody, Society of Manufacturing Engineers, One SME Dr., Box 930, Dearborn, MI 48121-0930; (313) 271-1500; fax (313) 271-2861.

Society for Information Display, International Symposium Seminar & Exhibition (SID '94), June 12-17. The San Jose Convention Center, San Jose, CA. Contact Joyce E. Farrell, SID '94 Conference Chair, Hewlett-Packard Laboratories, P.O. Box 10490, Palo Alto, CA 94303-0969; (415) 857-2807; fax (415) 857-4320; E-mail: Farrell@hplabs.hp.com.

CSI's NetSec '94, Network Security in the Open Environment, June 13-15. Sheraton Palace, San Francisco, CA. Contact CSI Conference Registration, 600 Harrison St., San Francisco, CA 94107; (415) 905-2626; fax (415) 905-2218.

Computer Modeling of Optical Waveguides and Components: A Hands-on Workshop, June 14-17. National Institute of Standards and Technology, Boulder, CO. Contact R. L. Gallawa, U.S. Dept. of Commerce, National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80303-3328; (303) 497-3761; fax (303) 497-3387.

Conference on Precision Electromagnetic Measurements (CPEM '94), June 27-July 1. Clarion Harvest House Hotel, Boulder, CO. Contact Donald B. Sullivan, Div. 847, National Institute of Standards and Technology, Boulder, CO 80303-3328; (303) 497-3772.

JULY

SPIE's Annual Meeting San Diego '94, July 24-29. San Diego Convention Center and Marriott Hotel and Marina, San Diego, CA. Contact SPIE, P.O. Box 10, Bellingham, WA 98227-0010; (206) 676-3290; fax (206) 647-1445; E-mail: Spie@mom.spie.org.

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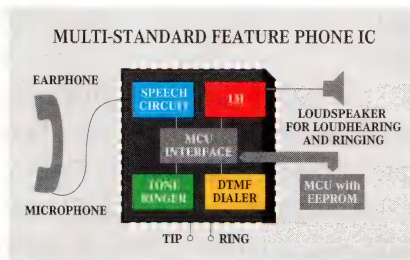
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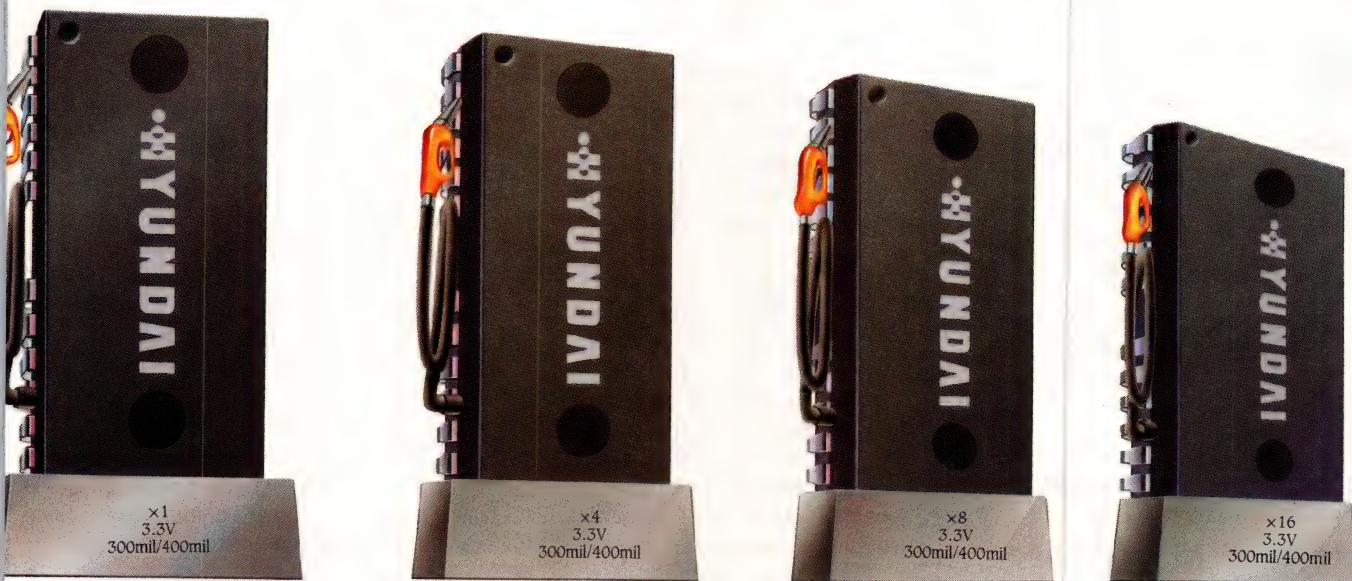


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	HY5116100A	5V	50/60/70	L, 2K/4K, SR	Q3, 94
	HY51V16100A	3.3V	60/70/80	L, 2K/4K, SR	Q3, 94
x4	HY5116400	5V	60/70/80	L, 2K/4K, WPB	Now
	HY5116400A	5V	50/60/70	L, 2K/4K, WPB, SR	Q3, 94
	HY51V16400A	3.3V	60/70/80	L, 2K/4K, WPB, SR	Q3, 94
x8	HY5116800	5V	70/80/100	L, 2K/4K, WPB	Q3, 94
	HY5116800A	5V	60/70/80	L, 2K/4K, WPB, SR, EDO	Q4, 94
	HY51V16800A	3.3V	70/80/100	L, 2K/4K, WPB, SR, EDO	Q4, 94
x16	HY5116160	5V	70/80/100	L, 1K/4K, WPB, 2C/2W	Q3, 94
	HY5116160A	5V	60/70/80	L, 1K/4K, WPB, SR, 2C/2W, EDO	Q4, 94
	HY51V16160A	3.3V	70/80/100	L, 1K/4K, WPB, SR, 2C/2W, EDO	Q4, 94

* Package: SOJ/TSOP II (standard/reverse)

* L-Low Power, 2K/4K-Refresh Cycle, WPB-Write Per Bit, SR-Self Refresh

2C/2W-2/CAS & 2/WE, EDO-Extended Data Out



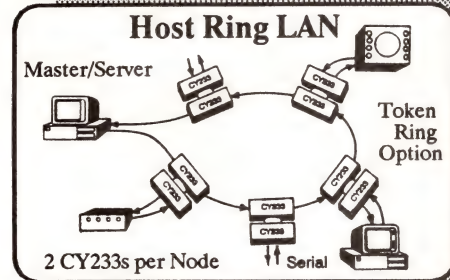
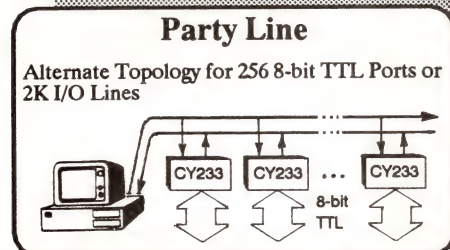
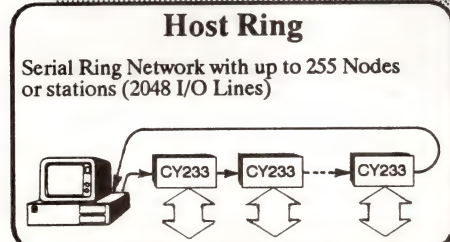
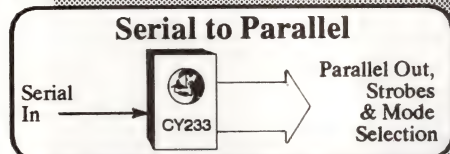
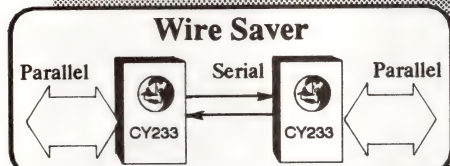
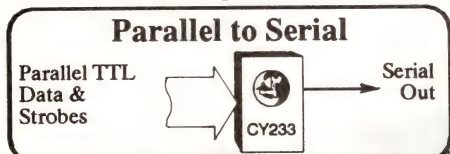
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EDITORIAL

AOKI-SAN

The first thing I heard about Aoki-san was that he is an accomplished "karate man": black belt or better. I'd just finished a course in basic Japanese and was looking for an informal Japanese tutor. One of his goals was to improve his English. I turned out to be a good candidate from Aoki-san's point of view because I speak a whole lot slower than most New Yorkers.

As luck would have it, our idea of conversing each other to fluency did not quite work. We both have busy lives. The time between sessions stretched from one month, to two, to four, etc. (No way to learn Japanese, take it from me).

But something more important than attaining fluency happened. We began to learn small but significant things about each other. He has three children, a son, Shohei, 15, and two daughters, Mai, 11, and Momoku, who is 9.

I ski, and at the age of 4, Aoki-san learned to ski in Hokkaido, the northernmost island of Japan. Like me, Aoki-san gardens. His favorite flower is clematis. Mine happens to be tulips, mostly because I like to see them push up after our long, white winters. We didn't agree on everything. In 1992, Aoki-san asked me who I favored in the presidential election. Clinton, I answered, because (unlike the Bush Administration) his advisers seem to appreciate the difference between exporting computer chips and potato chips.

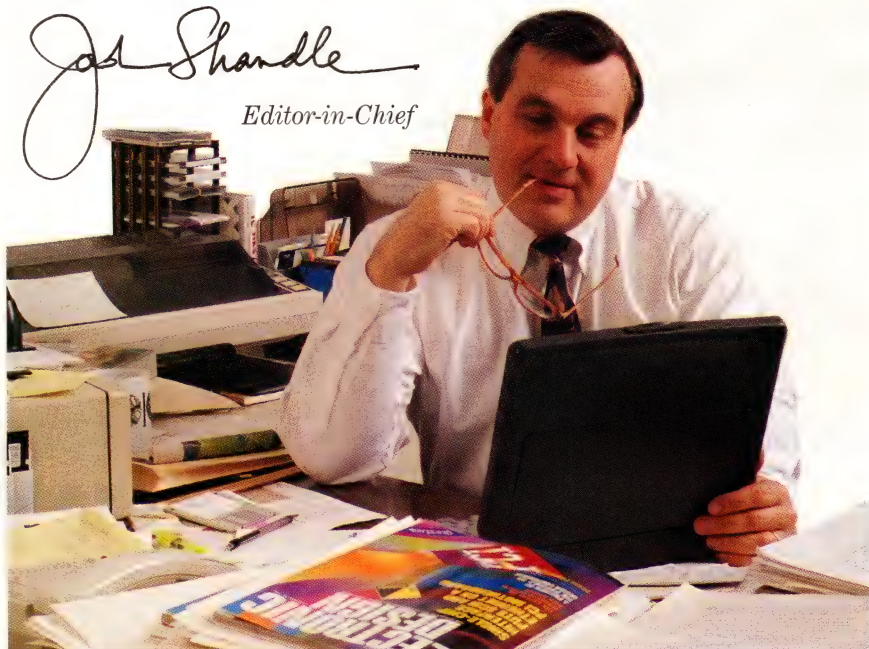
Clinton was elected and, if I'm to believe what I read in the newspapers nowadays, we have moved into a era of trade confrontation with Japan. Aoki-san and I haven't discussed this yet. But we are, I'm sure, a small part of the solution, as opposed to the politicians, who are a big part of the problem.

Politicians can only address problems within their sphere of influence. In other words, they can only pass laws and negotiate treaties. When a problem is deeply rooted in cultural differences, paper solutions aren't going to work.

During our infrequent visits, Aoki-san and I have taken some small steps in finding a cultural common ground. Things like: Shohei recently was admitted by a "good" high school in Japan (roughly equivalent to being admitted to a "good" university in the U.S.); and the quiet joy that clematis (and tulips) inspire when they bloom. Little things. Important things.

That small base of mutual understanding, when raised a few orders of magnitude, is what's needed. I wish the politicians good luck. But regardless of what they do or don't do, I can count Aoki-san as a friend.

Joe Shandle
Editor-in-Chief



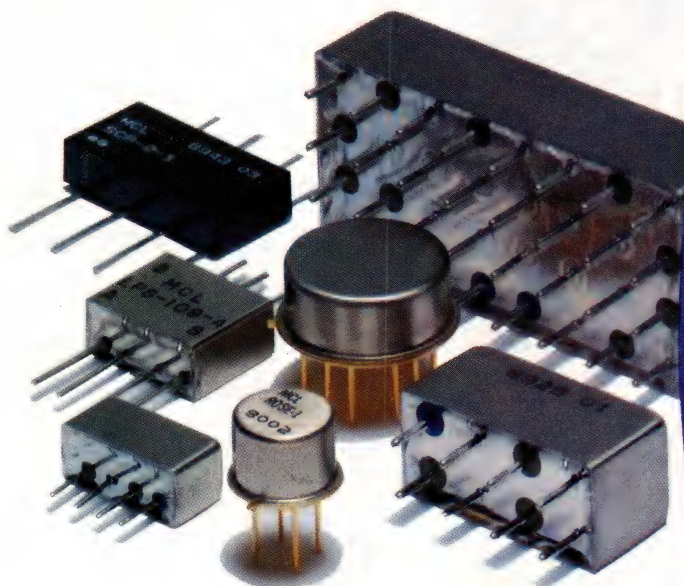
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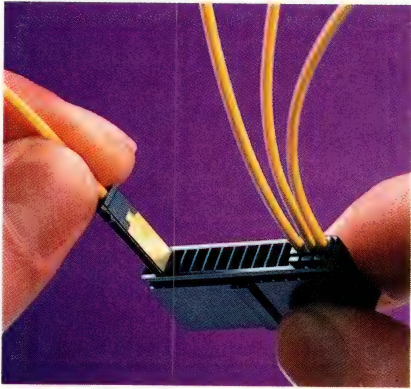
revenues, income, and earnings per share for more than 100 consecutive quarters since 1965.

Frankly, Ronald and I like to think there's a connection here."



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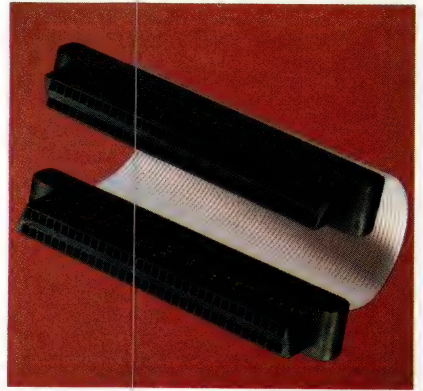
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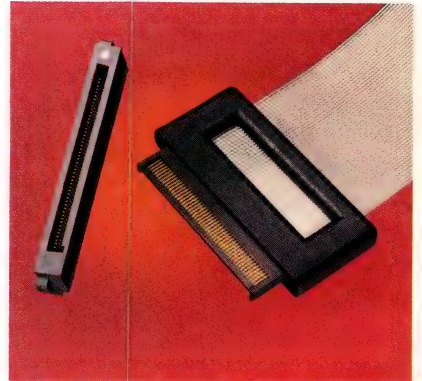
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Meritec's 68 position SCSI female-to-female cable assemblies are designed for applications requiring high speed, performance and reliability. Standard cable impedances of 85, 90, 95 and 100 ohms are available. The low profile connectors are terminated to FEP cable and overmolded for strain relief. Bused grounds are provided to customer designated pins. Terminations are mass soldered for high reliability. In addition to the female-to-female configuration, male-to-male and male-to-female versions are available on standard SCSI .050" x .100" spacing.

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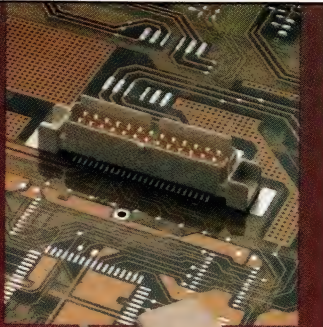
Memory Card Interconnect Systems



Meritec's new 50 position Memory Card Interconnect Systems provide I/O access to Elco PCMCIA card frames. Each system consists of an I/O card connector, which mounts to an Elco card frame, and a mating ribbon cable assembly. The basic design can be expanded to accommodate up to 68 circuits. The cable assembly portion of the system can be manufactured using a variety of cable configurations, including flat ribbon or round/oval. The assemblies are available with or without EMI/RFI electrical shielding. In addition to Elco frames, the system can be made to fit other manufacturers' frame configurations.

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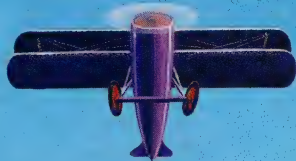
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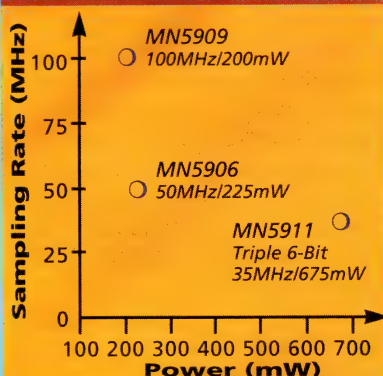
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TECHNOLOGY BRIEFING

DENSE ICs FORCE DESIGN-STYLE CHANGES

Chips based on deep submicron fabrication technologies are quickly outstripping the ability of most current design tools to provide accurate simulation results. Simulation tools now have to handle the parasitic and wiring RC effects once dismissed as negligible. And as power levels exceeding 20 W become conventional for CMOS circuits, tools must include power analysis as an intrinsic part of the circuit simulation.

It's essential for next-generation tools to take a top-down approach in order to provide a framework that considers circuitry, power, packaging restrictions, and other factors. In addition, tools should be able to analyze portions of the design against power and performance goals and constraints.

This issue's cover story—a joint effort between LSI Logic Corp., Milpitas, Calif., and Synopsys Inc., Mountain View, Calif.—features one approach that links the high-level design to the physical layout and provides back annotation directly to circuit synthesis tools. Although most design tool suites don't have such complete, other companies offer tools that verify circuit operation.

One such set of tools—TimeMill, PathMill, and PowerMill—developed by EPIC Design Technology Inc., Santa Clara, Calif., provides a suite of tools for hierarchical design and analysis. The tools verify IC functionality, timing, and power in both pre- and post-layout stages of a design. These tools also meld in with the new circuit design styles that mix dynamic and static logic and employ both dynamic simulation or static analysis. They hold the key to right-the-first-time designs.

In this era of short product life cycles (and thus short time-to-market needs), there just isn't enough time available in the design cycle to thoroughly exercise all test vectors on complex chips with a million or more transistors. Consequently, ensuring functional circuits at the design stage is essential. That requires attention to details, which in previous generations were lumped into third-order effects that could be ignored. Today, improper behavior not caught by gate-level simulations may force a significant redesign of the chip. In addition, overstressed areas of a chip could cause intermittent failure or early device breakdowns. But this must be balanced with overdesign that leads to inefficient use of the silicon or reduced performance.

Complex-chip design involves major issues that tools must deal with—complexity management (coordinating large design teams and the reuse of previously designed blocks), and power management (no longer trivial, as more attention must be paid to dynamically managing power). Some of the latest microprocessors employ dynamic power management that actually “shuts down” portions of the chips that aren't needed during a particular clock/instruction cycle, thus trimming the CPUs' power consumption.

As gate dimensions shrink, parasitic capacitances and resistances play an increasing role in determining top chip performance. But many older tools don't include the layout or interconnection distances on the chip. Such factors typically weren't accounted for when high-level circuit design tools were used because those tools usually use nominal or some other non-exact model to estimate circuit performance. New methodologies that couple the layout data back to the circuit design are key to delivering optimized designs.

As a result, rather than just setting a target for the desired functionality, today's designers also must include the chip power consumption and pin count. That's because consumption and pin count will determine the chip's package and the amount of cooling the host system needs to supply. Although systems can deliver the cooling, a nagging question might be “at what price” or how does it affect overall system reliability. By including these criteria in the design cycle from the beginning, circuits done right the first time will become more commonplace.



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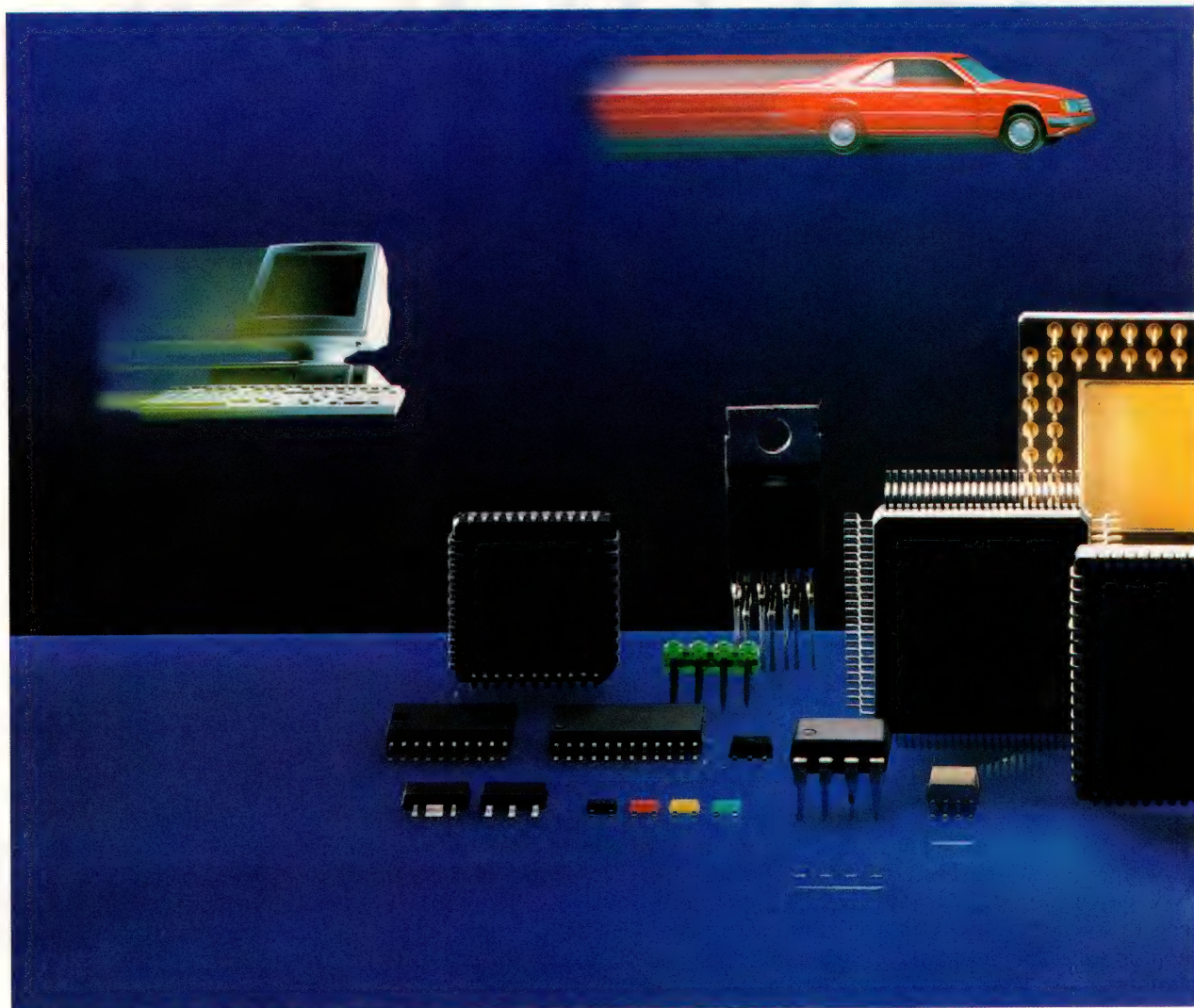


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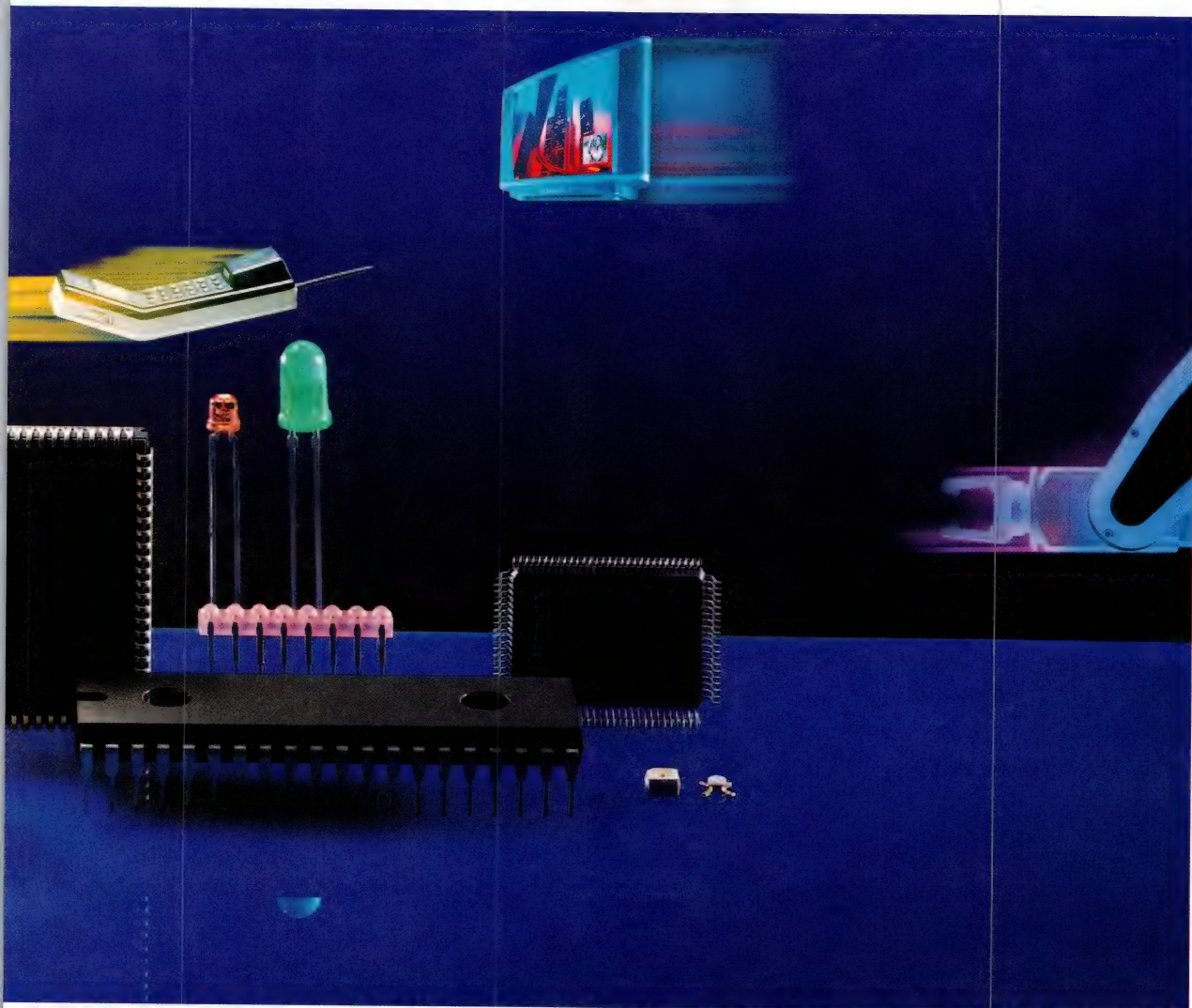
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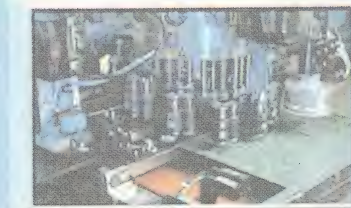
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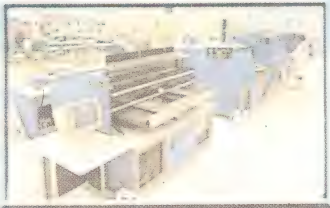
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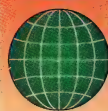
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TECHNOLOGY

NEWSLETTER



VOICE COMPRESSION MAKES ITS MOVE TO DSP ICs

With new personal-computer applications such as voice mail and voice annotation hitting the market, voice-compression technology becomes increasingly important. With that in mind, two companies, Analog Devices Inc., Norwood, Mass., and DSP Group Inc., Santa Clara, Calif., have joined forces to bring voice-enabled multimedia applications one step closer to reality. The DSP group will integrate its Truespeech voice-compression technology with Analog Devices' digital signal processors. Truespeech compresses voice files down to a small size, with negligible degradation. The compressed files allow data to be transferred easily from one user to another through an interoffice network or other means of transmission. This technology provides a low-cost solution for various applications, including voice mail, voice annotation, dictation, education, and training. Truespeech algorithms for Analog Devices' DSP ICs are expected to be available later this year. For further information, contact Al Haun of Analog Devices at (617) 461-3263. *CA*

PLZT CAPACITORS IMPROVE MCM DECOUPLING

Decreased package volume, improved speed, and greater design flexibility should follow from the creation of decoupling capacitors using thin films of lead-lanthanum-zirconate-titanate (PLZT). The capacitors, developed at Sandia National Laboratories, Albuquerque, N.M., are targeted for advanced packages, such as multichip modules (MCMs). That's because they can be more fully integrated into packages than ceramic capacitors. The films have very high dielectric constants ($\epsilon \approx 1000$) and excellent insulation resistance. They're fabricated by spin coating the film with a solution of metal alkoxides and carboxylates, and the capacitors are patterned using standard photolithography. For IC applications, the thickness of the PLZT dielectric is less than $1 \mu\text{m}$, which results in a large capacitance/unit area of about 10 nF/mm^2 . Thanks to their thin-film geometries and processing conditions, these capacitors can be directly incorporated into ICs and packages that require embedded components. For more information, contact Sandia's Duane Dimos at (505) 844-6385. *DM*

ADVANCES LOOMING FOR FLAT-PANEL DISPLAYS....

A joint development program between Coloray Display Corp., Fremont, Calif., and Sandia National Laboratory, Livermore, Calif., will attempt to develop an advanced flat-panel-display manufacturing technology. The three-year program is geared toward flat-panel displays with superior performance and lower manufacturing cost. Attention will focus on field-emission displays, and unique thin-film structures will be developed to aid in improving display performance and manufacturing yield. Alternate display fabrication techniques also will be investigated. Potential improvements in manufacturing technology could pave the way for improved U.S. competitiveness and participation in the global flat-panel-display market presently dominated by active-matrix LCD technology. For more information, contact Barry Schrader, Sandia National Laboratory Media Relations, at (510) 294-2447. *CA*

....AS WELL AS LARGE-AREA LCD FLAT PANELS

The production of future-generation large-area LCD flat panels will require high-speed and high-accuracy machines with submicrometer repeatability. Unfortunately, current machines used to print such flat panels experience a number of problems as the panel size and speed of the transport system are increased. With that in mind, the Lawrence Livermore National Laboratory, Livermore, Calif., and MRS Technology, Chelmsford, Mass., are working together to address this issue. They'll look to develop an appropriate manufacturing technology for active-matrix LCDs. The two-year cooperative R&D project will take place in three steps: magnetic modeling, transport-system design, and system isolation. All results will focus on the design of a new lithographic machine tool for next-generation larger active-matrix LCDs. For further information, contact the Livermore's public affairs office at (510) 423-3107. *CA*

NIST, IEEE EYE STANDARD FOR SENSOR INTERFACE

Efforts are underway by the National Institute of Standards and Technology (NIST), Gaithersburg, Md., and the TC-9 Committee of the Institute of Electrical and Electronics Engineers (IEEE) to define the requirements and potential benefits of a smart-sensor interface standard. The communications interface standard, though based on existing sensor technology, will be flexible enough to accommodate

FILTERS



dc to 3GHz from \$1145

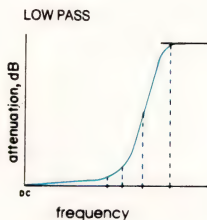
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low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz	Stopband, MHz	Model No.	Passband MHz	Stopband, MHz
	loss < 1dB	loss > 20dB		loss < 1dB	loss > 20dB
★LP-5	DC-5	8-10	★LP-250	DC-225	320-400
★LP-10.7	DC-11	19-24	★LP-300	DC-270	410-550
★LP-21.4	DC-22	32-41	★LP-450	DC-400	580-750
★LP-30	DC-32	47-61	★LP-550	DC-520	750-920
★LP-50	DC-48	70-90	★LP-600	DC-680	840-1120
★LP-70	DC-60	90-117	★LP-750	DC-700	1000-1300
★P-90	DC-81	121-137	★LP-800	DC-720	1080-1400
★LP-100	DC-98	146-189	★LP-850	DC-760	1100-1400
★LP-150	DC-140	210-300	★LP-1000	DC-900	1340-1750
★LP-200	DC-190	290-390	★LP-1200	DC-1000	1620-2100

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$32.95, SMA \$34.95, Type N \$35.95



Surface-mount, dc to 570MHz

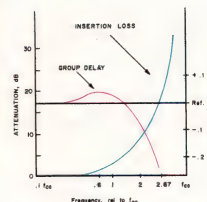
Model No.	Passband MHz	Stopband, MHz	Model No.	Passband MHz	Stopband, MHz
	loss < 1dB	loss > 20dB		loss < 1dB	loss > 20dB
SCLF-21.4	DC-22	32-41	SCLF-190	DC-190	290-390
SCLF-30	DC-30	47-61	SCLF-380	DC-380	580-750
SCLF-45	DC-45	70-90	SCLF-420	DC-420	750-920
SCLF-135	DC-135	210-300			

Price, (1-9 qty), all models: \$11.45

Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz	Stopband, MHz	VSWR	Group Delay Variations, ns
	loss < 1.2dB	loss > 10dB	Freq. Range, DC thru 0.6fco	Freq. Range, DC thru 2.67fco
★BLP-39	DC-23	78-117	1.3:1	0.7
★BLP-117	DC-65	234-312	1.3:1	0.35
★BLP-156	DC-94	312-416	0.3:1	1.1
★BLP-200	DC-120	400-534	1.6:1	1.1
★BLP-300	DC-180	600-801	1.25:1	0.4
★BLP-467	DC-280	934-1246	1.25:1	0.2
★BLP-933	DC-560	1866-2490	1.3:1	0.09
★BLP-1870	DC-850	3740-6000	1.45:1	0.05

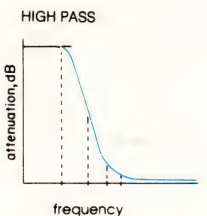
Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95
NOTE: ▲ -933 and -1870 only with connectors, at additional \$2 above other connector models.



high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband, MHz	Passband, MHz	VSWR	Model No.	Stopband, MHz	Passband, MHz	VSWR
	loss < 40dB	loss < 20dB	Pass-band Typ.		loss < 40dB	loss < 20dB	Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	★HP-400	DC-210	210-290	395-1600
★HP-50	DC-20	20-26	41-200	★HP-500	DC-280	280-365	500-1600
★HP-100	DC-40	40-55	90-400	★HP-600	DC-350	350-440	600-1600
★HP-150	DC-70	70-95	133-600	★HP-700	DC-400	400-520	700-1800
★HP-175	DC-70	70-105	160-800	★HP-800	DC-445	445-570	780-2000
★HP-200	DC-90	90-116	185-800	★HP-900	DC-520	520-660	910-2100
★HP-250	DC-100	100-150	225-1200	★HP-1000	DC-550	550-720	1000-2200
★HP-300	DC-145	145-170	290-1200				

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

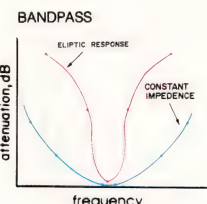


bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max (MHz)	3 dB Bandwidth Typ. (MHz)	IL > 20dB at MHz	Stopbands I.L. > 35dB at MHz	Model No.	Center Freq. MHz	Passband I.L. loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000	★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000	★IF-30	30	25-35	1.9 & 210	DC-330
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000	★IF-40	42	35-49	2.6 & 300	DC-400
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000	★IF-50	50	41-58	3.1 & 350	DC-440
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000	★IF-60	60	50-70	3.8 & 400	DC-500
						★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95, SMA \$42.95, Type N \$43.95

Constant Impedance, 21.4 to 70MHz



Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

NOTE: ★Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.

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future technologies and permit sensor integration compatible with many interface hardware implementations. This endeavor will occur in three phases, the first of which is a Smart Sensor Interface Standard workshop to be held at NIST from March 31 through April 1. The workshop will address issues of emerging sensor technology and industry needs. Other topics of discussion include the establishment of general communication-protocol and data-transfer formats, selection of several hardware implementations and development of a public-domain library or software drivers for them, selection of standard connectors for smart sensors and transducers, and a summary of information in the IEEE Draft Standard. All final phases, resulting in a completed standard, are expected to be finished in the next few years. For more information, contact Tammie Grice at NIST at (301) 975-3883. *CA*

TOUCH SCREEN WORKS THROUGH 2-IN. GLASS

A projected-capacitive input technology can sense touch through a 2-in.-thick sheet of glass. The technique, developed by Moonstones Designs Ltd., Brentford, Middlesex, United Kingdom, works by projecting a voltage field out from a transparent glass sensor with discrete touch zones on its surface. Though it typically resides over a CRT, the sensor also can sit behind graphics or other objects, allowing users to obtain information simply by touching a picture. When a touch occurs, minute changes in the voltage field are detected and the touch is assigned to one of the sensor's pad areas. Pad size can be as small as 0.25 in.². The projected-capacitive input technology is available in the U.S. from MicroTouch Systems Inc., Methuen, Mass. For more details, call Jay Waldron of MicroTouch Systems at (800) MICROTOUCH or (508) 659-9000. *RN*

MULTIMEDIA COMMUNITY SETTLES ON DATA EXCHANGE

Sharing of multimedia information across various platforms and applications has been made possible by the Interactive Multimedia Association (IMA). That's because they selected the Open Media Framework (OMF) interchange and Apple Bento container formats as the underlying technologies for its Data Exchange Recommended Practice (DERP). The IMA, Annapolis, Md., made the selections after a detailed technical evaluation, which was part of its Compatibility Project. The DERP's goal is to improve the quality of the titles, clip media, and multimedia data available. To accomplish such a task, the portability of data across platforms and applications had to be improved. The OMF interchange format will give developers and end users what they need to create, share, and distribute different types of multimedia data. The OMF format is a publicly available format that uses Apple's Bento as the means by which it stores and accesses objects. The DERP is now being drafted by the IMA and is expected to be released by the end of this year. *DM*

EXPERIMENTAL CMOS POWERPC RUNS AT 2.0 V

By bringing the operating voltage of a PowerPC 601 microprocessor down to 2.0 V, power dissipation can be reduced three-fold without noticeable performance loss. That's what researchers at IBM Microelectronics, Essex Junction, Vt., achieved with an experimental PowerPC 601 chip developed from a standard 3.6-V, 0.6- μ m CMOS part. The chip was modified for low-power operation without altering its circuits and masks. Moreover, yield wasn't affected. A manufacturing fabricator processed the ICs using standard tools with the standard product mask set. The experiment aimed to demonstrate a potential migration path for early entry into low-power applications. More details on this development will be unveiled at the VLSI Technology Symposium, June 6-11, at the Hilton Hawaiian Village in Honolulu. Call Ms. Melissa Widerkehr at (202) 986-1137 for additional conference information. Contact John Bertsch of IBM at (802) 769-8845 about the device. *RN*

MCT BUILDING BLOCKS SIMPLIFY POWER DESIGN

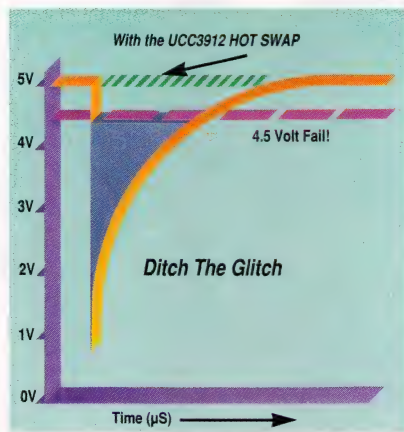
A new generation of power electronic building blocks (PEBBs) with MOS-controlled thyristors (MCTs) may simplify the design of power-conversion and conditioning circuits. Under a joint effort that's part of a two-year grant from the U.S. Government's Technology Reinvestment Project (TRP), Harris Semiconductor, Melbourne, Fla., and the Electric Power Research Institute (EPRI), Palo Alto, Calif., will research process, package, and drive technologies, as well as the integration of power transistors and drive circuits into PEBBs. They will work to develop a high-power, p-channel MCT handling up to 2.5 kV with more speed and 30% higher turn-off rating than traditional models. Also in the works are high-power, n-channel MCTs that will handle up to 4 kV, featuring half the losses and twice the speed of existing insulated-gate bipolar transistors (IGBTs). These developments will result in a broader range of applications for PEBBs. Roughly 2000 free prototype PEBBs will be distributed to designers in a variety of fields, including industrial, university, and military organizations. For more information, contact Harris at 1-800-4-HARRIS. *CA*

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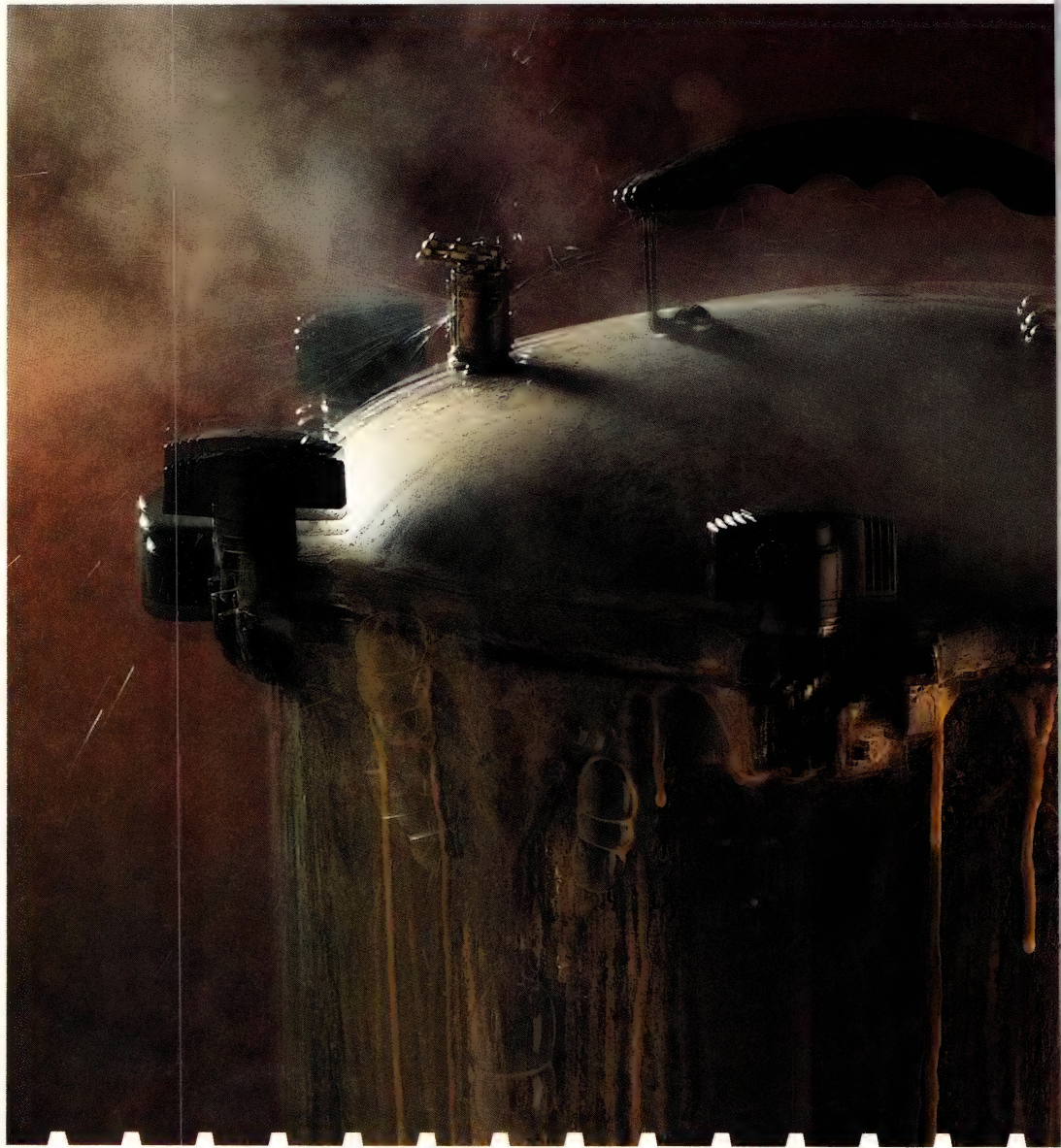
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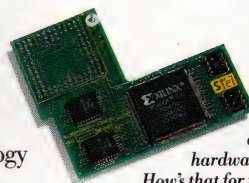
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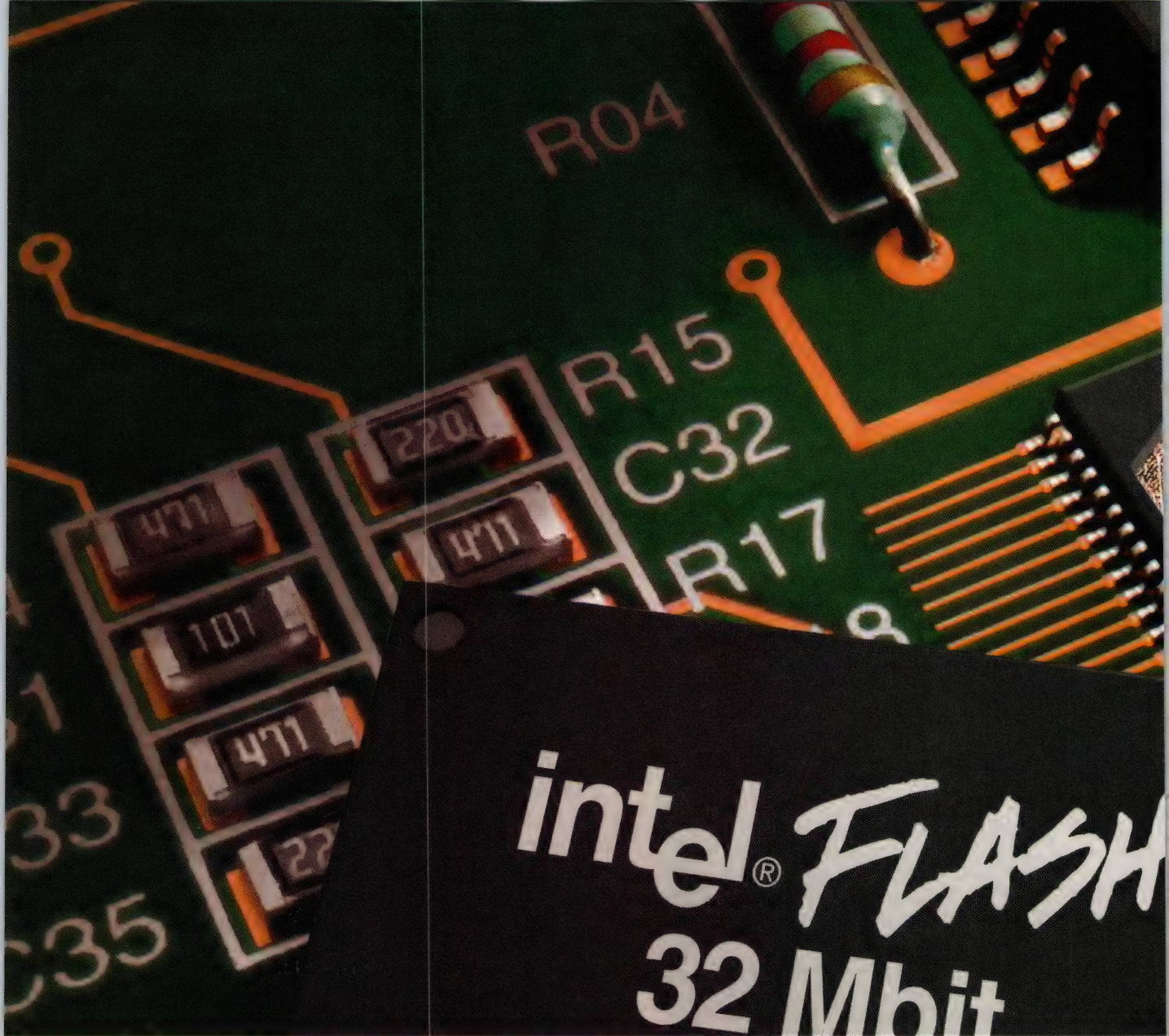
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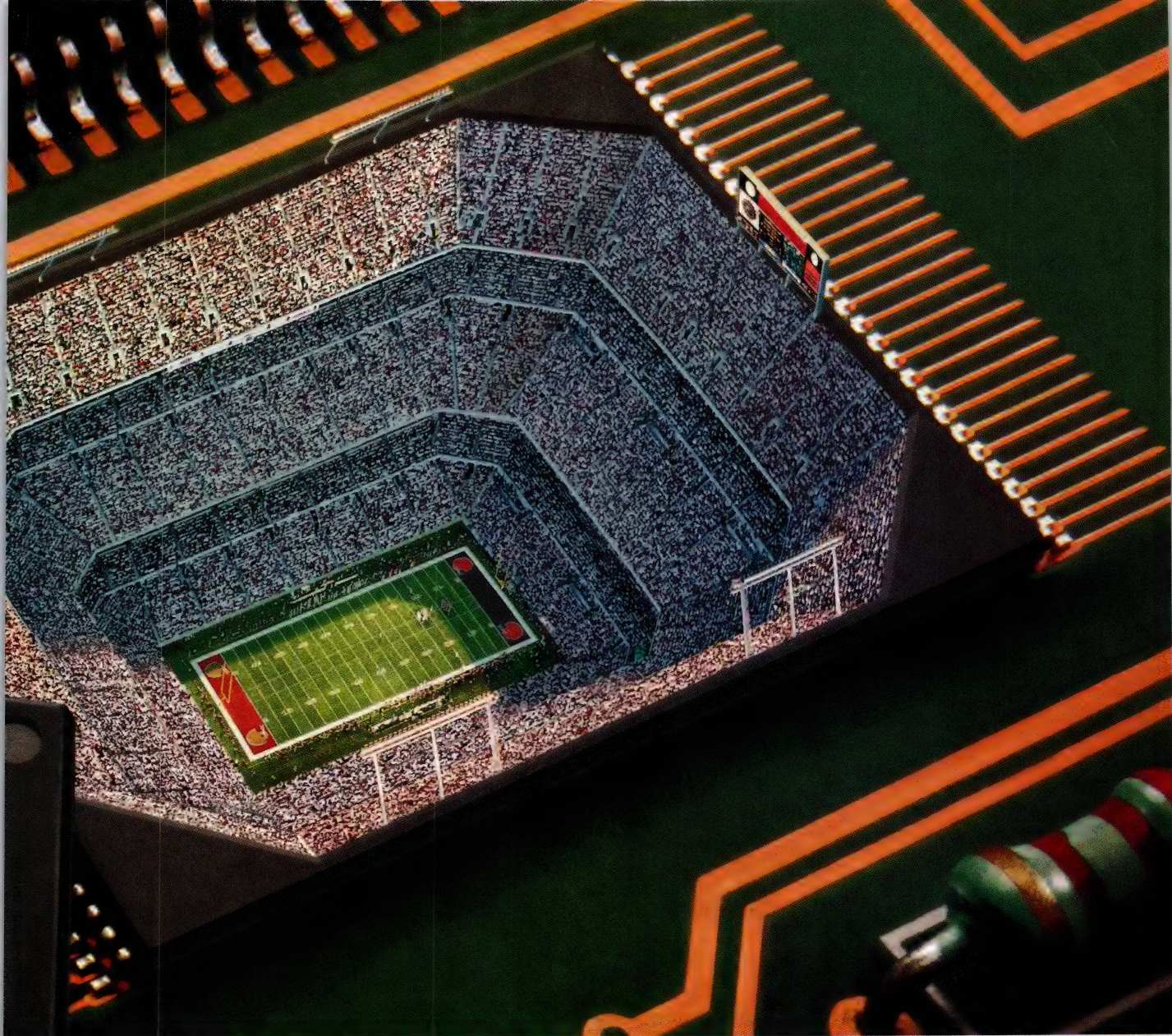
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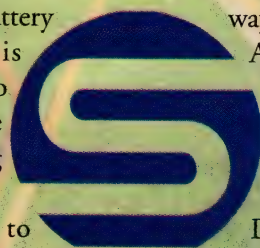
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READER SERVICE 135

SOFTWARE-COMPATIBLE x86 SUPERSCALAR CHIP SET ACCELERATES PERFORMANCE

Staying compatible with the x86 instruction set while delivering performance matching or exceeding that of the Intel Pentium microprocessor is no trivial challenge. Similarly, delivering the solution at a market price that's well below the Intel part places another equally difficult challenge in front of any supplier trying to compete for CPU sales.

By taking a "divide and conquer" approach to their superscalar architecture, designers at NexGen Microproducts Inc., Milpitas, Calif., created a radically different architecture in their Nx586 microprocessor chip set. It implements the x86 instruction set using a translation scheme, in which x86 instructions are first converted internally into an intermediate RISC code that's executed by the Nx586-processor architecture.

Outwardly, NexGen Mi-

croproducts' Nx586 chip set functions as a binary-compatible x86 microprocessor. However, rather than integrate all of the logic on one chip, NexGen designers divided the architecture by moving the floating-point unit off the chip, much like the older architectures of the 386/286/86 microprocessors (see the figure).

One reason for the split came as the result of a market analysis. The analysis showed that a very high percentage of system users rarely needed floating-point computations.

The chips will be manufactured in a 0.5- μ m CMOS process and operate with clock speeds of 60 or 66 MHz. About 3.5 million transistors are employed by the CPU and about 700,000 transistors are employed for the math unit. The novel architectural approach produces performance gains or losses, depending on the benchmark

used.

For example, using the PowerMeter 1.81 and Norton SI 7.0 benchmarks, performance of the 60-MHz CPU decreases by 7% and 14%, respectively. On the other hand, using the Landmark 2.0, Byte 2.4 desktop, and Byte 2.4 notebook benchmarks leads to performance gains of 8%, 28%, and 28%, respectively. These results were run on an ALR Evolution V Pentium PC.

The split architecture does rule out pin compatibility with the Pentium microprocessor. As a result, NexGen Microsystems' designers had the "freedom" to define a more optimal pinout. Their choice: a trio of 64-bit buses to ensure the CPU isn't kept waiting for instructions or data.

The first bus is dedicated to the second-level cache interface, the second bus provides access to the main memory and I/O system, and the third bus is dedi-

cated to the coprocessor interface (the first coprocessor is the Nx587 floating-point unit, but others can be added).

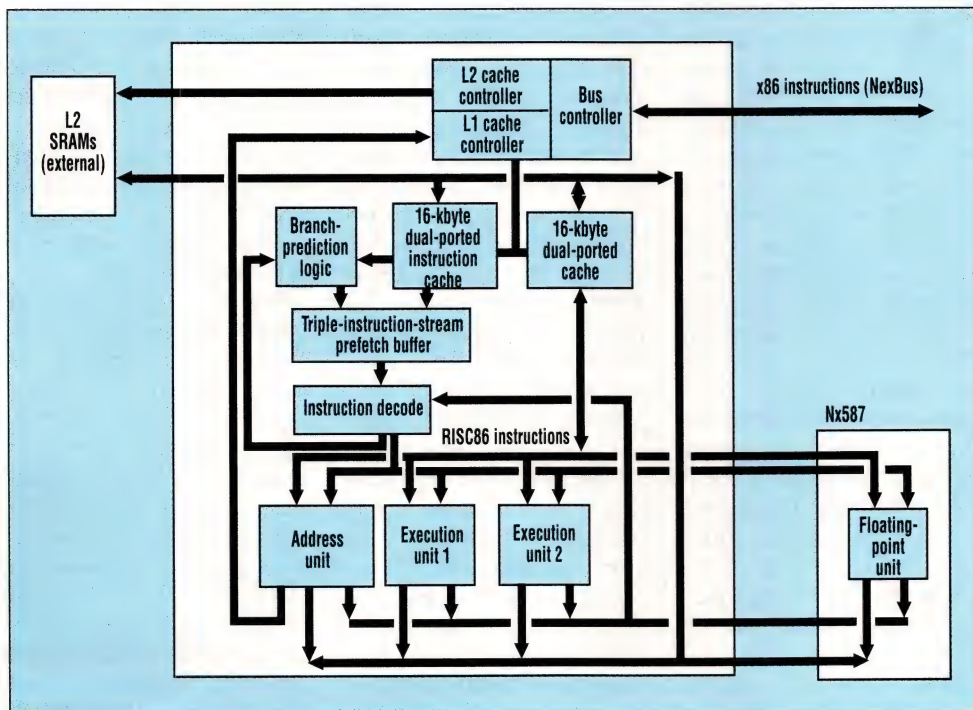
The Nx586's internal microarchitecture that actually executes the instructions incorporates many approaches that differ drastically from the Pentium microprocessor's internal implementation. For starters, NexGen Microsystems' designers created a RISC microarchitecture they dubbed RISC86. The RISC86 engine contains its own instruction set, which is run using a superscalar execution unit, branch-prediction logic, large on-chip caches, and 64-bit data buses.

To speed the system-level data transfers, a second-level cache controller that can address up to 1 Mbyte of memory was integrated on the integer-processor chip. This integration eases timing requirements for external cache memories and also reduces potential bus conflicts with system accesses.

The RISC86 engine executes a proprietary RISC instruction set that was specially designed to directly support x86 instructions. At the same time, it obeys the RISC implementation principles of fixed-length encoding, regularized instruction fields, and a large register set.

A key block within the microarchitecture is the decoder/scheduler unit. It translates the x86 instructions into RISC86 instructions, and also dispatches the RISC86 instructions to the chip's other units.

The decoder/scheduler, which handles exceptions and records instruction termination and retirements, also manages the processor resources needed by the in-



structions. Part of the unit includes one of the most advanced branch-prediction blocks used in a microprocessor. That block accelerates branches and performs speculative execution and tracking of multiple instruction streams.

One key function that's performed by the decoder/scheduler is that it keeps a continuous record of the processor state. The tracking is needed to guarantee precise exception handling and to ensure that the processor maintains consistent and coherent states, even when backing out from an execution of a wrongly predicted speculative instruction stream. This processor state includes all of the architecturally visible registers and flags, all of the additional physical registers used for mapping, and a variety of queues and buffers employed to reduce dependencies and accelerate key operations.

To make such a record-keeping capability practical, a large register set was placed in the decoder/scheduler block. Using a "register renaming" scheme, the eight x86 registers are remapped into a portion of a register space larger than what's specified by the x86 instruction set. The decoder/scheduler manages the mapping by time-stamping instructions and assigning and keeping track of the RISC86 registers being mapped to x86 registers.

Such a process prevents instructions from being stalled by the lack of available registers and assures that each instruction has the correct data from previous instructions. This overall scheme allowed NexGen designers to employ simpler execution units because only the de-

coder/scheduler manages the complexity.

To feed the on-chip execution units, NexGen Microsystems includes double the amount of Level 1 cache than that found on the Pentium—16 kbytes each for the data and instruction caches. Moreover, the chip's Level 2 cache controller allows for fast cache-line refills while relaxing the access-time requirements for off-chip SRAMs. That reduces the cost of the secondary cache.

As mentioned earlier, the second part of the trick was to deliver the CPU at an "affordable" price. The 60-MHz CPU is priced at \$460 each in 1000-unit quantities, while the 66-MHz version will sell for \$506. That's about one-third less than the Pentium, as of early

March. The floating-point coprocessor sells for \$128.

Because the CPU includes the secondary cache controller and uses moderately-priced SRAMs, overall motherboard implementation costs are lower than for Pentium-based motherboards. Consequently, designers should be able to configure systems that sell for less than \$2000. To make motherboard designs simple, NexGen designers also crafted a system-logic chip to support the CPU—the NxVL provides all of the basic motherboard logic and both ISA and VL-bus interfaces. A version with a PCI-bus interface is in development.

For more information, contact Dana Krelle at (408) 435-0202.

DAVE BURSKY

THE IS-54B TDMA DIGITAL CELLULAR STANDARD GAINS MORE SUPPORT WITH A PUSH FOR SILICON DEVELOPMENT

With another major semiconductor manufacturer adding its support, the time-division multiple-access (TDMA) standard will gain added momentum in its quest for digital-cellular-market leadership in North America. NEC Electronics, Mountain View, Calif., plans to build a highly integrated chip set targeted for cellular telephones that conforms to the IS-54B TDMA standard. Under a recently released agreement, DSP Telecom (DSPT), Plainsboro, N.J., will develop the entire baseband technology of the chip set that will be manufactured and distributed by NEC.

The TDMA standard competes directly with the

IS-95 code-division multiple-access (CDMA) standard. The two competing systems, which were assigned interim-standard (IS) numbers by the Telecom Industry Association (TIA), have been unleashed within the marketplace to vie for dominance. IS-54 TDMA technology improves on current analog cellular techniques by transmitting several compressed, digital audio channels over the same bandwidth previously used for a single conversation. IS-95 CDMA technology is a more complex (and currently more expensive) spread-spectrum technique, but it provides for 5 to 10 times more traffic within a given spectrum than TDMA

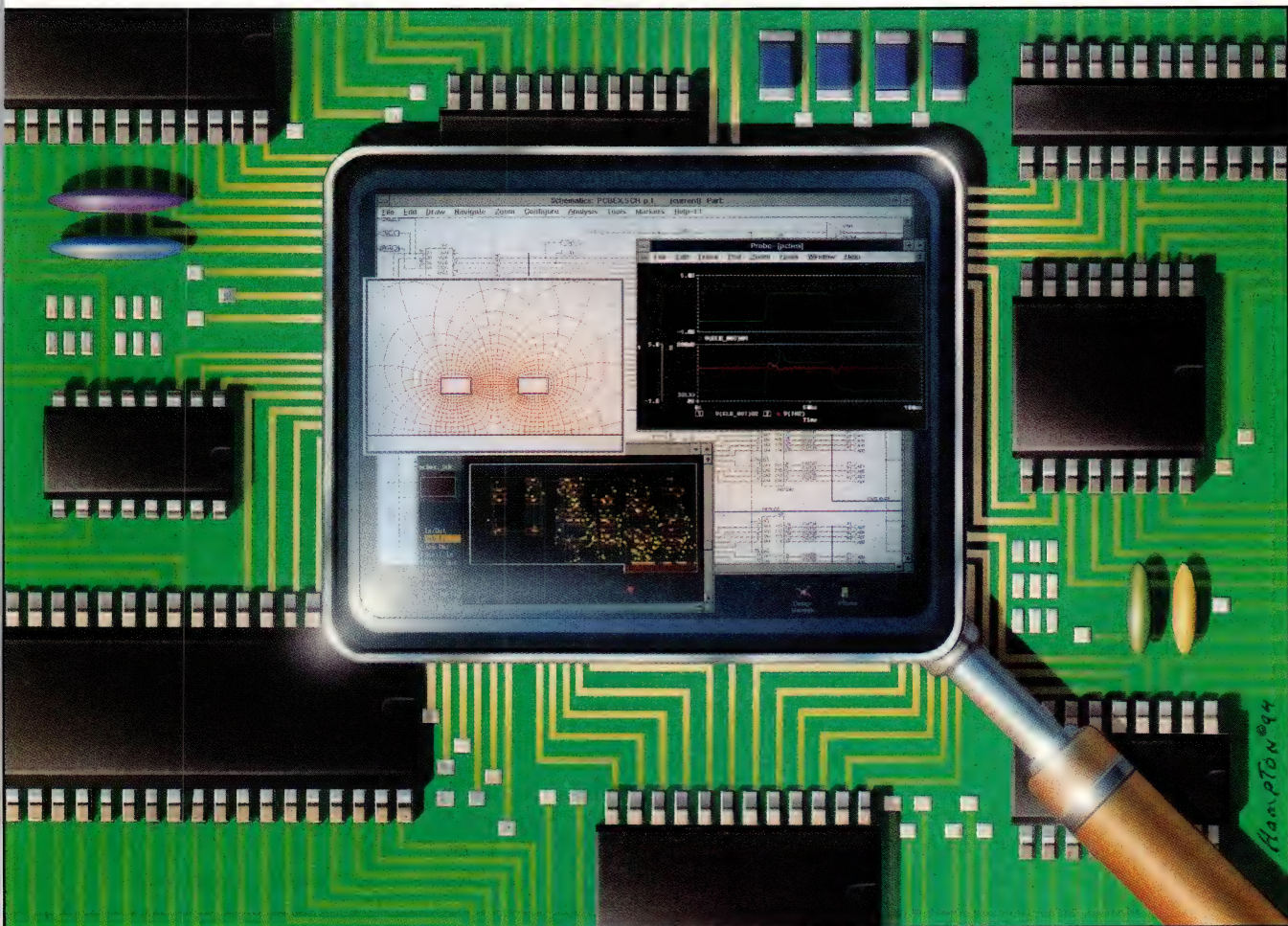
technology.

Even though CDMA technology offers higher absolute traffic capacity, NEC's decision to support the less-sophisticated TDMA technology was influenced by current market trends in North America. Over the past year, 16 of 25 major U.S. metropolitan cities adopted TDMA as their digital cellular standard. In an effort to relieve the crowded existing analog Advanced Mobile Phone Service (AMPS) channels, most of these cities are working toward having digital service in place by early 1995.

With delivery of NEC's IS-54B silicon anticipated for early 1995, selection of potential beta-site customers is nearly complete and chip development is underway. According to Rick Kepple, marketing manager for NEC, the agreement will capitalize on the strengths of both participants by using NEC's marketing and manufacturing infrastructure and DSPT's extensive background in digital speech processing. NEC is a leading supplier of DSP hardware for a wide spectrum of applications while DSP Telecom is a pioneer in the arena of application-specific digital-signal processing technologies and possesses in-depth expertise in cellular telephony.

While no description of specific technologies to be used for the project has been released, it's a good bet that NEC's new digital-signal processor showcases some of the high-performance features that will be embedded within the cellular chip set. Designated the μ PD77017, the DSP chip features a 33-MIPS Harvard-architecture CPU with pipelined instruction and data paths, a 16-bit fixed-

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point processor; and low-power 3-V operation.

Initial efforts are focused on quick roll-out of the IS-45 chip set, but Kepple says NEC and DSPT haven't ruled out the possibility of co-developing other products. NEC is currently evaluating the marketplace for a chip set that would implement IS-54+, an en-

hanced TDMA standard capable of supporting advanced cellular features like digital control channels and short-message channels. Such features would give cellular telephones capabilities similar to those offered by the Integrated Services Digital Network (ISDN).

Though TDMA has taken

a strong foothold in North America, the competition is far from over. If consumer use of cellular technology continues to grow, the increased channel utilization offered by the TDMA standard may only offer temporary relief for the crowded airways.

Kepple also says that NEC hasn't ruled out the

possibility of developing a CDMA cellular chip set. He indicates that NEC is taking a wait-and-see position at the moment, until it can be determined whether increasing traffic density and other factors will give the CDMA standard a chance at better market penetration.

LEE GOLDBERG

SUPER-FINE E-BEAM LITHOGRAPHY IS THE KEY TO 110-GHZ SILICON PHOTODIODES

By using super-fine-line electron-beam lithography, a team of researchers at the University of Minnesota's Department of Electrical Engineering developed silicon-based detectors that can operate at a frequency of up to 110 GHz. These are the fastest silicon photodiodes reported to date. Potentially, such an advance can make fiber-optic communications up to 50 times faster than currently available technology.

The secret to designing and fabricating these fast and tiny photodetectors is miniaturization, explains Stephen Chou, an engineering professor and team leader of the project. To make the detector, professor Chou's group developed a high-performance electron-beam lithography machine. Their machine is one of only a few that can produce line widths as small as 100 Å (0.01 µm).

Chou notes that the significance of this work is partly due to its use of silicon, the semiconductor material that's used to build the majority of ICs available on the market. While some commercially available detectors can operate at a frequency of up to 60 GHz, they're fabricated

from compound semiconductors, such as gallium arsenide, and aren't always easily compatible with applications utilizing silicon ICs.

The new photodetector consists of an interdigitated array of gold fingers deposited on a silicon substrate (*see the figure*). When a light beam slips through the grid and hits the silicon, electrons are freed, generating an electrical signal that indicates light was detected.

Spacings between the fingers had to be extremely small to minimize the time the electrons spend generating a signal. The larger the spacings, the longer it takes the photodetector to operate.

Because the device is fab-

ricated on silicon material, it may be possible to use biCMOS or other process technologies to fabricate additional circuits on the same chip. For example, signal-conditioning as well as logic circuits can reside on the very same chip as the sensor.

Chou says the breakthrough is so dramatic that measuring the device's speed required the efforts of a second group of researchers before Chou's group set up its own femto-second-measurement facility. The performance measurements conducted by the second group were led by Thomas Hsiang, an electrical-engineering professor at the University of Rochester and senior scientist at Rochester's Laboratory for

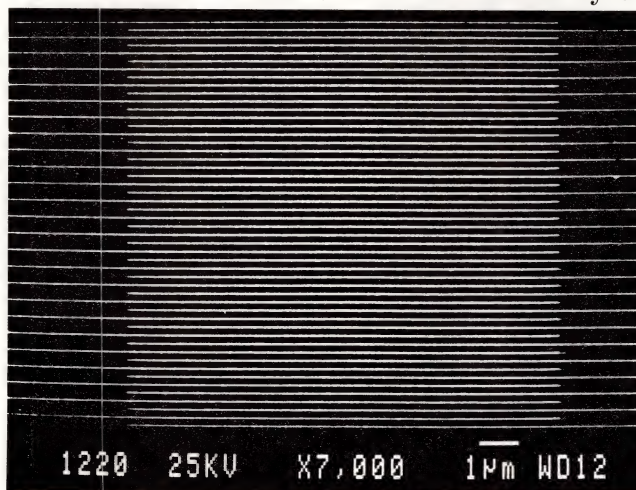
Laser Energetics. Hsiang's group is one of few in the world able to do such measurements.

Hsiang studied the detector by sending it powerful laser pulses lasting less than a trillionth of a second. The laser pulses were generated by a tunable titanium-doped sapphire laser that acted much like a very fast strobe camera.

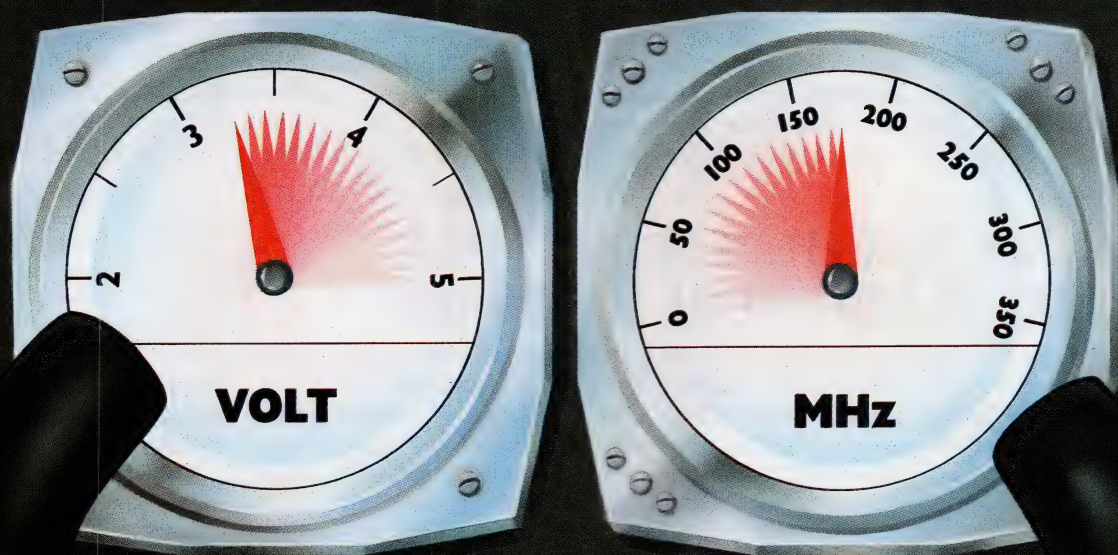
In the process of studying the detector, it was discovered that signals from red light generate a slower signal than violet light because red light penetrates silicon deeper. The deeper the light goes, the deeper the electrons are liberated and the further they must travel to get out of the silicon and hit a gold electrode.

Significant increases in the performance of high-speed networks and data transfers between computer components are anticipated as this technology finds its way into commercial applications. Besides obvious data-transmission applications, the device is an extremely sensitive ultraviolet and microwave detector. This capability makes it a sensitive, rugged, and compact detector for remote-sensing applications.

In another configuration, the device can be stimulated to emit a very narrowband signal. This al-



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lows it to be used as a good microwave frequency reference source.

Also working on the project were graduate students Mark Lue Liu of Minnesota, as well as Sotiris Alexandrou and Chia-Chi

Wang of Rochester. The Minnesota work was supported primarily by the Packard Foundation, with additional support from the National Science Foundation (NSF), the Army Research Office, and the Semi-

conductor Research Corp. At Rochester, support came from NSF, the U.S. Department of Energy and the New York State Energy Research and Development Authority. The work was reported at the

1993 Device Research Conference in Santa Barbara,

For further information on the project, contact Deane Morrison at the University of Minnesota at (612) 624-2346.

LEE GOLDBERG

NEURAL-NET ALGORITHM REUSES FPGA RESOURCES TO ADD VIRTUAL HARDWARE

By exploiting the in-system reconfigurability of RAM-based field-programmable gate arrays (FPGAs), an artificial neural-network method can increase the number of neurons by 500% without quintupling the amount of hardware used. The scheme, proposed by researchers in the Department of Electrical and Computer Engineering at Brigham Young University, Provo, Utah, divides the back-propagation algorithm in the neural network into three stages that are executed sequentially.

The FPGAs are first used to execute one stage, then reconfigured to execute the second stage, reconfigured again to run the third stage, and finally reconfigured back to their starting state. Such reuse increases the number of hardware neurons that can be implemented in one FPGA by 500%.

Dubbed the run-time reconfigurable artificial neural network (RRANN), the scheme divides the back-propagation algorithm into three stages: feedforward, back propagation, and update. The feedforward stage takes input patterns and propagates them backward through the network, assigning an activation (output) to every neuron according to a weighting algorithm. The back-propagation stage finds the output errors and propagates them backward through the network to find errors for neurons contained in hidden layers.

After every non-input neuron is assigned an error value, the update stage uses activation and error values from the previous two stages to compute the amount by which the weights should be changed and then updates the weights.

The RRANN scheme uses one FPGA as a global

controller and an FPGA for each neural processor (see the figure). Each neural processor, in turn, contains one, three, or six neurons, depending on the algorithm option selected at startup. The controller, which is mainly responsible for sequencing the execution of the local hardware subroutines on the neural processors, also supplies key data to the neural processors (input patterns, for example).

Each neural processor executes local hardware subroutines under the control of state machines. A local RAM associated with each neural processor stores the weights and target output data, and serves as a scratch pad memory to buffer net and error values.

To utilize the hardware efficiently, RRANN employs bit-serial hardware to execute the mathematical computations. Lookup tables are used to implement

the activation function and its derivative.

Tests were done using PC-hosted cards developed by National Technology Inc. Each card has sockets that hold up to eight FPGAs.

A variety of algorithms, some using as few as six neurons to those employing over 20, were evaluated for neural-network performance and for overhead issues related to reconfiguring the FPGAs.

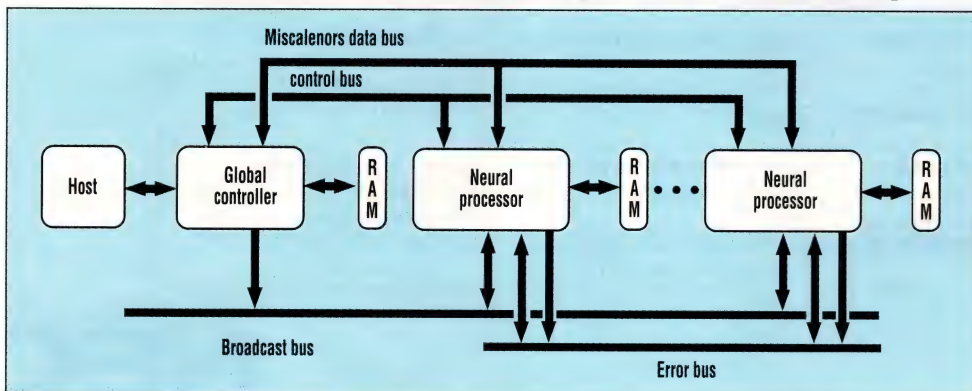
With the FPGA reconfiguration time assumed to be about 7 ms, six hardware neurons were effectively implemented in one FPGA, and the system ran at a frequency of up to 14 MHz. By adding several pipelining improvements, researchers expect the circuits to operate at a frequency of up to 40 MHz.

In its learning mode, the system performed from 94,600 to about 568,000 weight updates per second, depending on various configuration options tried by researchers.

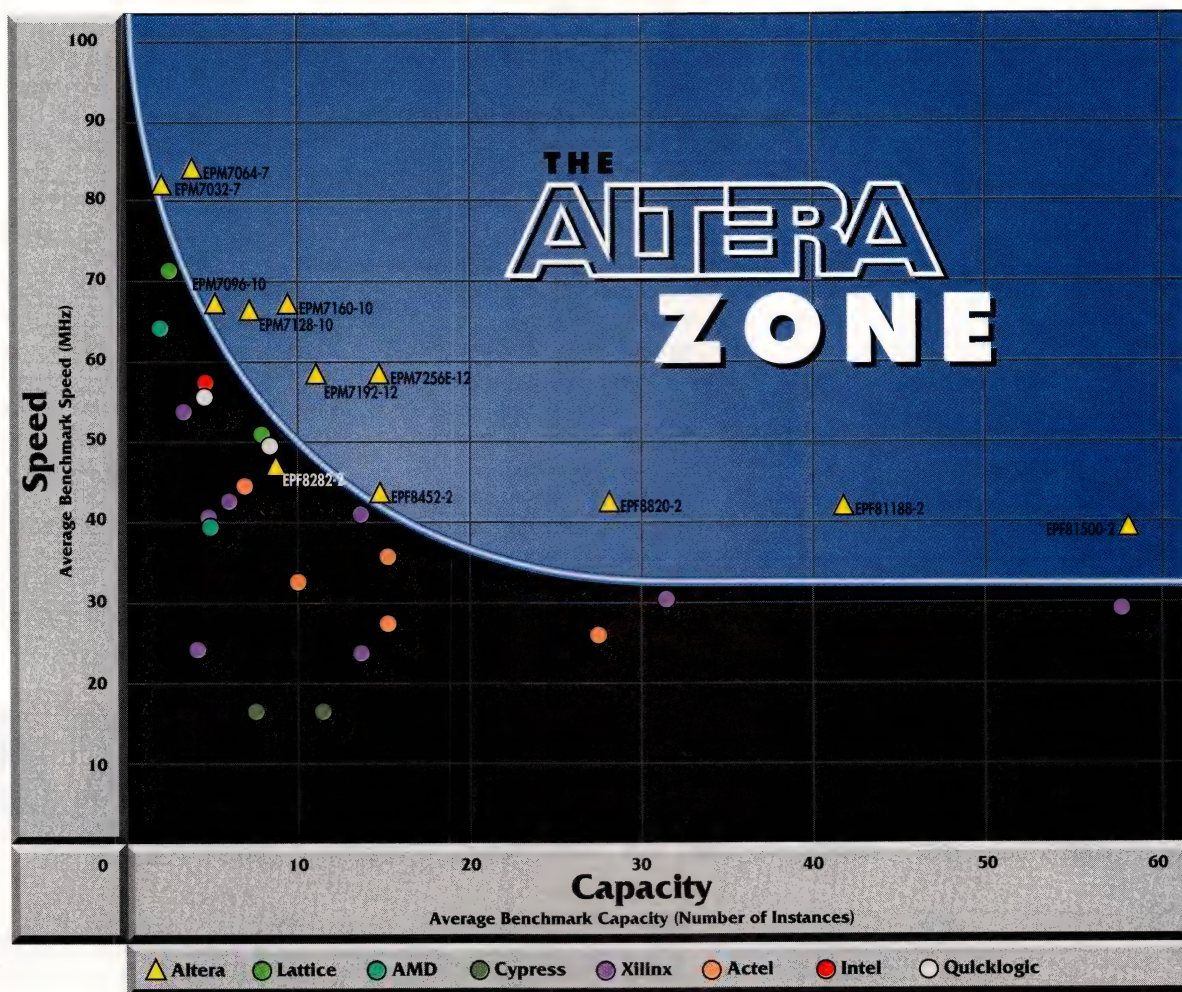
Full details of the RRANN scheme will be released at next month's IEEE Custom Integrated Circuits Conference, May 1-4 at the Town & Country Hotel, San Diego, Calif. To obtain CICC registration information, contact Widerkehr and Associates at (202) 986-2166.

For additional information on the RRANN, call Brad Hutchings at (801) 378-4012.

DAVE BURSKEY



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LOW-COST COPROCESSOR BOARD USES MASSIVELY PARALLEL PROCESSING TO ACHIEVE 800 BOPS

It's not much bigger than a breadbox, but a coprocessor board made up of massively parallel processors can supply 800 billion operations/s (BOPS). The Micro-Grain Array Processor (MGAP), under development at Pennsylvania State University, University Park, Pa., employs massively parallel processors that ultimately will combine high performance with low cost.

Designed for engineering workstations, the board can potentially put mainframe-like power into a desktop system. The prototype board, which cost \$10,000 in parts, is 100 times faster than the university's main-

frame computer in certain applications. The current processor configuration resides in a Sun workstation chassis.

"The key to the board is its simplicity," says Dr. Mary Jane Irwin, professor of computer science and engineering at Penn State's College of Engineering. "In the MGAP, we combine a large number of very simple processors in a parallel configuration to supply the power."

The MGAP's design doesn't lend itself to all applications, though. It's most suited for signal and image processing, and is well equipped to handle problems encountered in mete-

orology, computational biology, and astronomy.

For example, in image processing, the MGAP can speed up the task of locating objects and defining their edges. It does this by executing many simple, yet rapid, calculations, and then putting the aggregate together to come up with an image. Because the board can speed up the compression and transmission of image data, it's also suited for real-time imaging technologies, such as video teleconferencing.

Because Penn State's researchers aren't part of the commercial business world, they're trying to determine the next step. "Building

processor chips and boards is a good way to prove a concept and educate graduate students in what's needed to design and create these next-generation computers," says Irwin. "Building the processor is just the first step. We also needed to write a compiler that will work with our primitive processors, and then the programs that will run most efficiently on the system."

The design goal was to pack as many chips onto the board as possible, with each containing the maximum number of digit processors. Each digit processor can handle one write and two read operations per cycle. By having many processors working together—16,384 in the MGAP prototype—massively parallel computations can be achieved.

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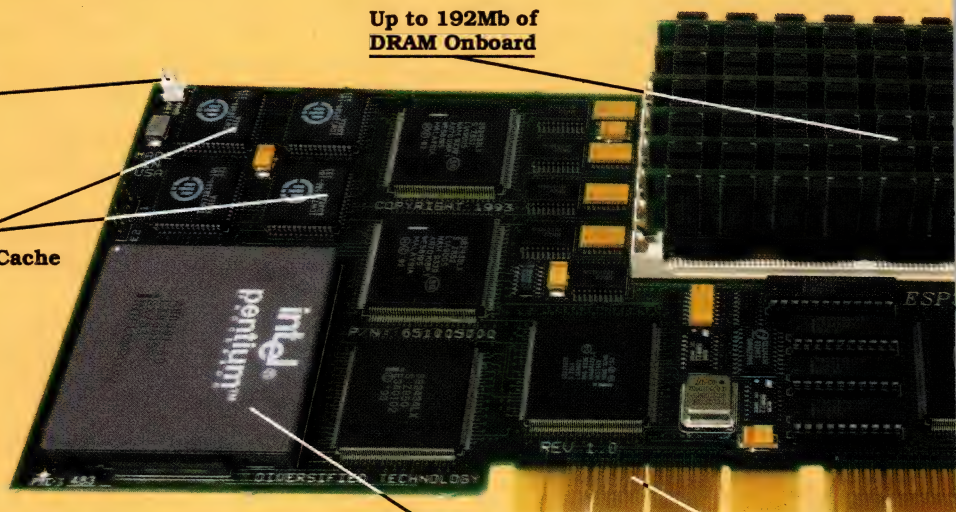
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The design of the digit-processor chips was heavily influenced by cost. Because inexpensive computing power was the primary concern, a standard 1.2- μ m CMOS process was chosen for fabrication, with some performance being traded off for lower cost. "If we had refabricated the processors using the same exact mask for the chips, but with 0.8- μ m technology, we could've gotten twice as many processors on the board, but at a higher cost," claims Irwin. "If we redesigned the mask, we think we could reduce the size by another 50%."

The board was designed so that most of the necessary memory for program development didn't reside on the board. This also freed

up pc-board space to include more digit processors.

The board's software is written in C++, an object-oriented language that's employed in many engi-

neering workstations. Irwin says, "We would have liked to design our own language. But that would have gone against the flow. Most people are using some form of C." The compiler and

software reside in the host workstation.

For more information about the MGAP, contact Dr. Mary Jane Irwin at (814) 865-1802.

RICHARD NASS

TECHNOLOGY IN ACTION

State-of-the-art design approaches aren't necessarily limited to adult electronic designers. This was clearly evident at a recent scholastic scholarship competition awards presentation held March 30 at the Anaheim Marriott in California. There, the winning teenage students were recognized for achievements in scientific innovations.

At the competition, sponsored by the Duracell Bat-

tery Co. and the National Science Teachers Association, a first place prize of \$20,000 in U.S. Series EE savings bonds was awarded to Tracy C. Phillips, a 17-year-old Long Beach High School student of Peter J. Rubino, Long Beach, N.Y.

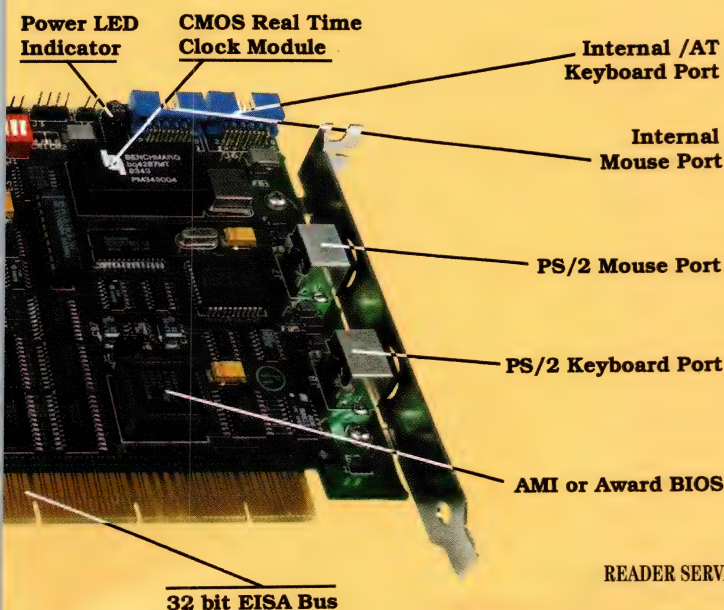
She invented "Money Talks," an electronic wallet that reads paper-money denominations for the blind. After placing a bill into the wallet, the device

states the denomination's value. It works by using an IR light emitter/detector that lets varying amounts of light pass through the bill's printed patterns, identifying key distinguishing points. Light passed through each point is converted to an electrical signal. A digital logic circuit then matches codes, identifies the bill, and activates a voice-synthesis chip. Power comes from four AAA batteries.

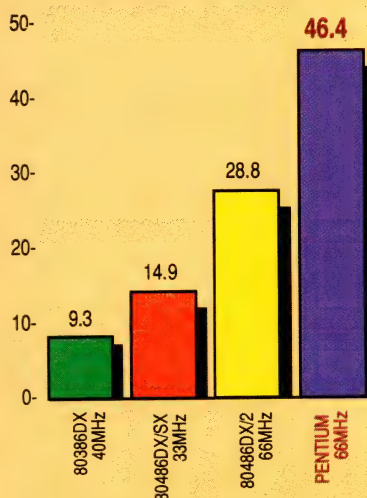
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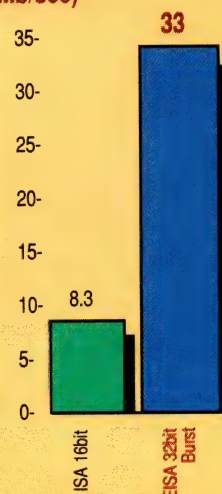
Computer Architecture



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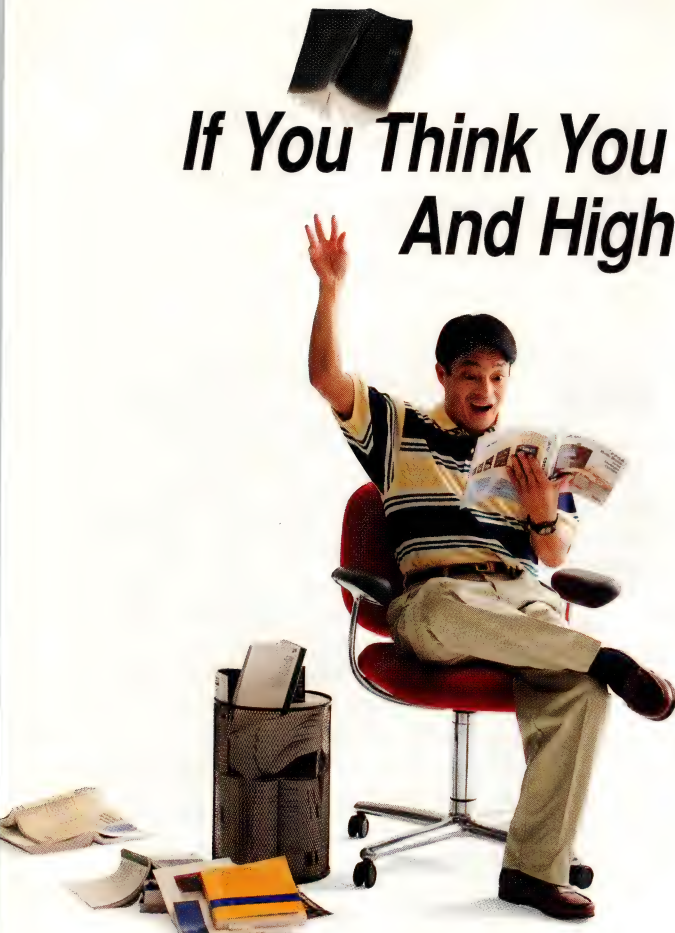
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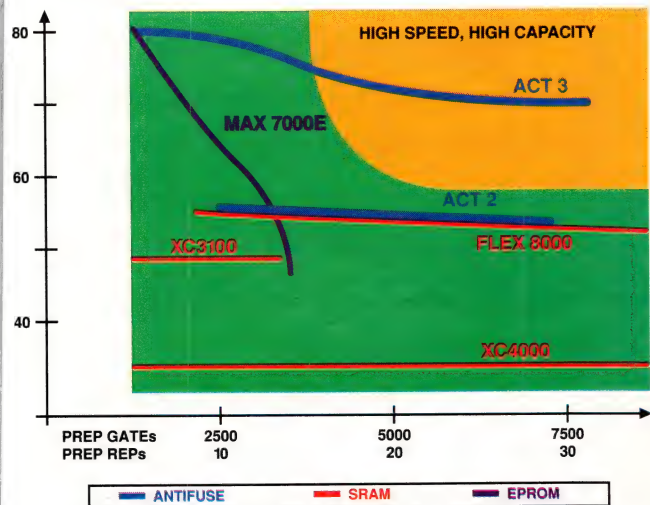
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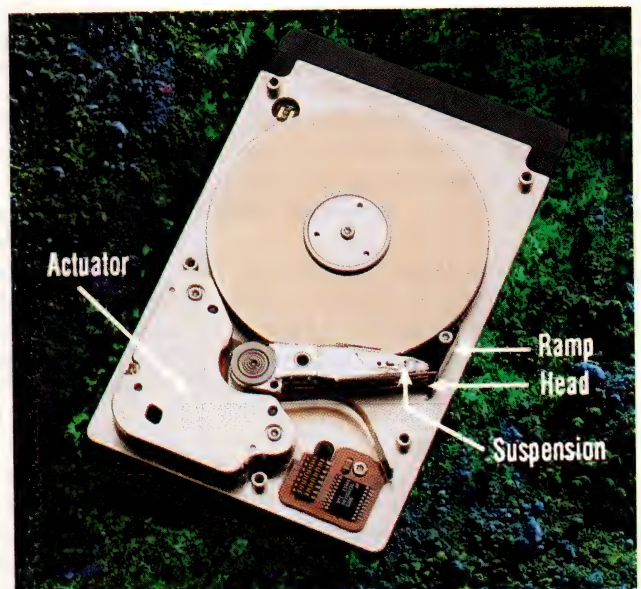
H

ard-disk-drive manufacturers are poised to pounce on the exploding market of notebook and handheld computers. While the same engineering concerns over higher capacities and smaller form factors still exist for disk-drive designers, there are now other issues to deal with, primarily because of the portability of the new systems.

Two of these issues are lower power and increased reliability. Lower-power consumption is driven by the need to get longer life from the batteries. The reliability factor comes into play simply because portable systems take more abuse from everyday travel than their stationary desktop brethren.

A third issue is that the drives aren't designed solely for embedded applications anymore. With the mounting popularity of the PCMCIA specification, removable drives are starting to appear. The first wave of PCMCIA-based disk drives were intended primarily for secondary storage because of their relatively low 40- and 80-Mbyte capacities. Typically, users would store their applications on the system's primary storage subsystem (an embedded disk drive), and use the PCMCIA drive to hold the data files (such as a spreadsheet, database, or word-processing document) so those files can be transferred easily from system to system. Having the files on a removable disk also increases security, because if the system can't be moved, the files can still remain with the user.

Lately, some PCMCIA drive announcements are changing that primary-secondary storage paradigm. The first to break the 100-Mbyte barrier, and thus become a candidate for primary storage, was Maxtor Corp., San Jose, Calif., with its MobileMax 105-Mbyte drive. The two-platter drive fits a PCMCIA Type III form factor (10.5-mm high), as do all of the



1. HEAD SLAP in a disk drive can be eliminated by the dynamic ramp-loading technique, as used in the drive from *Intégral Peripherals*. When the drive is powered down, the head moves to the outside diameter of the disk and rests on the ramp.

SMALL FORM-FACTOR DISK DRIVES

current PCMCIA-based hard-disk drives. Maxtor's announcement was quickly followed by similar releases from a host of disk-drive manufacturers, including MiniStor Peripherals Corp., San Jose, Calif., which recently announced a 128-Mbyte drive.

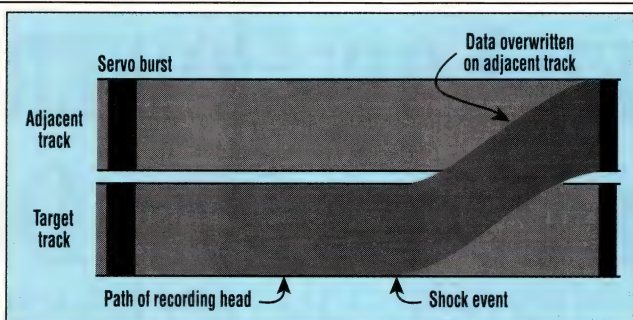
Intégral Peripherals Inc., Boulder, Colo., one of the pioneers in 1.8-in. disk drives, will ship a 170-Mbyte drive later this quarter. In addition, the company claims it will offer a 210-Mbyte model sometime in the second half of the year. This will be followed by a 100-Mbyte Type II drive, which solves many of the slot-contention issues. For example, one Type III drive requires two stacked Type II slots—currently the configuration of choice for most systems. By going to a Type II form factor (5-mm high), users will still have one Type II slot available for other peripherals, such as a local-area-network (LAN) or modem card. A Type II drive contains enough room for just one platter.

The reliability factor is key to the success of PCMCIA-based disk drives. "Head slap," which happens when a drive is dropped, is a prominent problem in the many contact start-stop-type drives available. Occurring at about 200 to 300 G, the head lifts off the disk and slams back down, digging a hole in the landing zone of the media. Also, the corners of the head can chip with the debris being distributed onto the disk. Such events can result in permanent data loss.

To put these shock levels into perspective, 500 G is roughly equivalent to a 1-ft. drop onto a hard table, or from table height onto a carpet. A 1500-G shock is approximately equal to a drop from table height onto a tiled-concrete floor.

DYNAMIC HEAD LOADING

One way to avoid head slap is to employ a dynamic head-loading technique, such as the one used in the drives developed by Intégral. With dynamic head loading, the head rests on a ramp, so it never touches the media. Hence, there's no head slap.



2. A SHOCK INCURRED on an operating drive can cause the head to inadvertently shift from the target track to an adjacent track. It's possible for the data on the adjacent track to be overwritten and lost.

When power is removed from the drive, the heads are moved to the disk's outer diameter where a ramp structure lifts the head off the disk (Fig. 1). The head actually comes to a rest beyond the disk's outer diameter, once again preventing head slap.

As the disk spins up to full speed, the head lands on a fully-developed cushion of air (called an air bearing) and never touches the disk. "In addition to increasing the non-operating shock specification, dynamic head loading offers an unlimited start-stop capability," claims Jim Morehouse, executive vice president of R&D at Intégral. "This is important because drives of this type are subject to lots of starts and stops to save power."

In contact start-stop drives (drives that don't employ dynamic head loading), the head lands on the inside diameter of the disk (in the landing zone). As the disk spins down, the head comes to rest on the disk. These drives typically are specified for a mean-time-between-failures (MTBF) at about 80,000 start-stops.

A high non-operating-shock specification also requires an effective actuator clamp to keep the heads off the disk. One approach is to employ an inertial lock, which resembles that of a seat-belt mechanism. It locks the heads off the disk during any shock. The shock actuates the lock so that the stronger the shock, the stronger the lock.

Operating shocks can be detrimental to the data on the drive. Today's small form-factor drives usually employ an embedded-servo technology to position the heads over a desired track. This system reads the infor-

mation written at the beginning and end of each sector for the correct positioning. But the servo information can't be read while the system is reading or writing data. Consequently, if a shock is incurred after the positioning data is read, the head may lose its positioning until the next series of servo information is read. This could induce the head to stray outside the current track boundary onto an adjacent track, causing the

data on those adjacent tracks to be overwritten (Fig. 2).

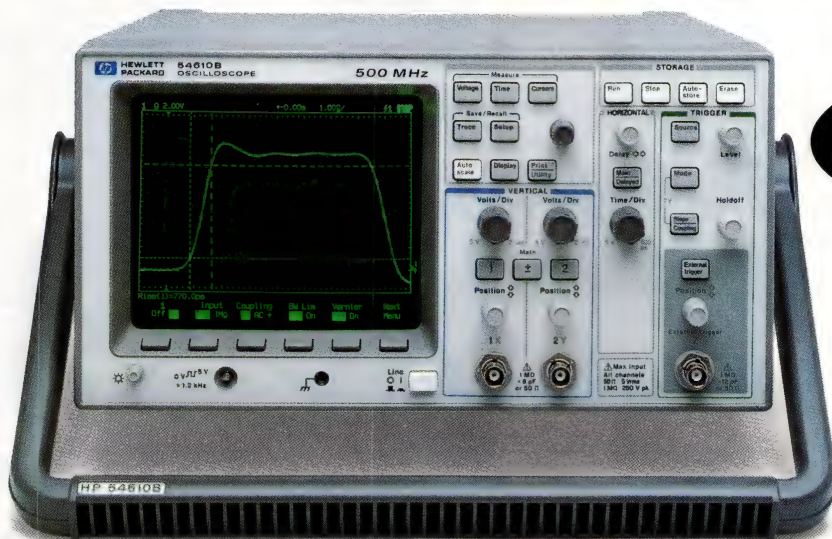
Most drives employ similar techniques to resist operating shock. In the Z direction, the heads actually touch down on the disk at around 100 G. But an operating drive is obviously mounted within the system (whether it's embedded or plugged into a PCMCIA slot), so there's some built-in protection. The system's case supplies about a 3X protection improvement. In other words, if the drive can withstand 100 G or operating shock, the system can be hit with a 300-G shock without causing any damage to the drive.

INCREASED SHOCK LEVELS

The operating-shock specification is incorporated in the SafeRite technology developed by Seagate Technology Inc., Scotts Valley, Calif. The SafeRite sensors, which are employed in all of the company's products including the PCMCIA-based drives, can detect a shock and halt a write operation before the recording head is knocked far enough off track to lose the current data and destroy adjacent tracks. The sensor continues to monitor the environment until stability is regained, then allows the write function to be executed. The operation is completely transparent to both the user and the host system.

The type of motor employed in a disk drive also affects the drive's shock resistance. Ball-bearing-based motors are employed in most of the small form-factor drives, although some manufacturers are moving to hydrodynamic designs. Maxtor is one company making lots of progress with the hydrodynamic spindle

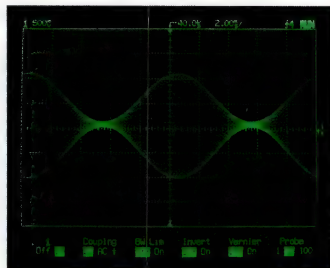
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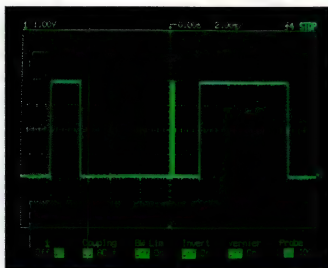
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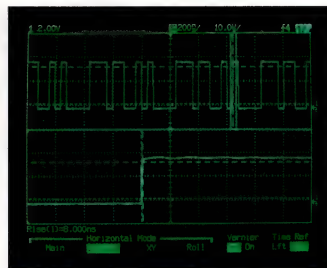
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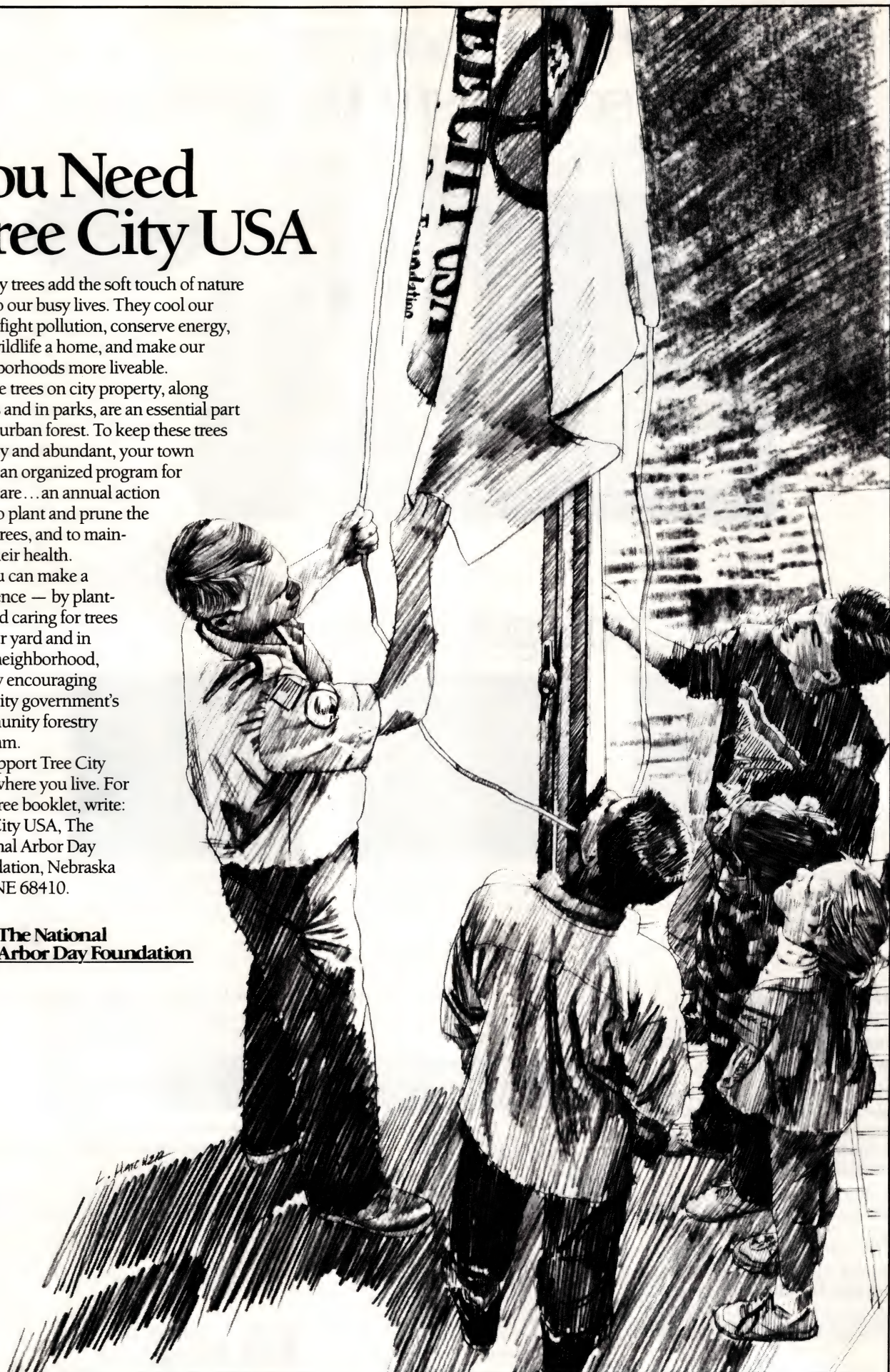
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motor. In fact, the motor is used in its MobileMax drive.

The idea for the hydrodynamic motor originated in the consumer-electronics industry. It's a low-profile in-hub motor, which means that the rotor and windings are situated inside the motor. The whole unit then fits in the center of the disk, rather than having the rotor positioned underneath the casing.

The hydrodynamic motor eliminates point-to-point metal contacts that exist in a traditional ball-bearing motor. As a result, if the drive receives a severe shock, the point-metal contact that can deform the casing is removed. Such a deformity may not cause a data loss since, in many cases, the drive's internal error-recovery procedures are able to restore the data. But as the number of deformities accumulate, the drive's performance will decrease. That's because the firmware is forced to perform more error-recovery algorithms to recover the data. Eventually, the drive won't be able to access a particular track.

"Because of the hydrodynamic motor's durability, we increased the non-operating shock specification of our drive to 600 G," says John Hagerman, vice president of mobile products at Maxtor. "In addition, because the motor has no ball bearings, it's extremely quiet. We spec the drive at 28 dBA, but in practice, it's actually much better than that. And it's still significantly better than our 1.8-in. competitors." The hydrodynamic technology has no effect on the drive's spin-up time, though.

KEEP THE POWER DOWN

Holding the power draw of the 1.8-in. disk drive down to an acceptable level is a big concern for drive designers. One way to reduce the power is to power-down parts of the drive that aren't being used. This feature must be implemented in the drive's firmware, but it does introduce a trade-off with response time, calculated as the access time plus the latency time.

A disk drive can possess various power modes. The most power, typically greater than 2 W, is expended when the drive first spins up. Executing read and write commands and

seeking (moving the head to a particular spot on the disk) also requires a relatively large amount of power, which is around 1.5 to 2 W. In the idle mode, some of the electronics are turned off, but the disk keeps spinning. The response time from this mode ranges from 0.1 to 1 second, depending on the drive. In the contact start-stop drive, the head is either biased against the inner crash stop or simply floating on the disk's surface. In dynamic head-loading drives, the head is unloaded during the idle mode.

STOP THE DISK

The biggest power savings is derived by stopping the disk from spinning as often as possible. In the standby mode, the disk stops spinning and some of the electronics are shut down. The typical response time from this mode ranges from 1.5 to 5 seconds and the power draw is typically under 50 mW. When set to the sleep mode, the drive needs a reset before it can accept any commands. Some drives call for a hardware reset, while others can take a software reset without requiring any special software. Power consumption is lowest in the sleep mode, which can drop to 5 mW in some cases.

Many drives have a built-in timer that puts the drive into the various low-power modes after a preset time delay. But quite often, the preprogrammed delay is longer than expected. That's because the drive has a finite number of starts and stops before a failure occurs. Each spin-up wears the media slightly. Consequently, some 2.5-in. drives won't spin down more than once per minute, while some 1.8-in. models won't spin down more than once every 20 seconds.

One part that can reduce the power draw is the IMP62C540 single-chip read-channel device. It dissipates 10% less power than the previous-generation part. Because all the needed logic fits into one 64-pin thin quad flat pack, the chip is suited for 1.3-, 1.8-, and 2.5-in. drives. It's integrated servo demodulator features a serial addressing scheme that requires fewer control lines than competitive read-channel solutions. In addition, the IMP62C540 operates at

a data rate of 40 Mbits/s.

Another issue that will eventually affect the mass-storage subsystem is the industry's eventual move from 5- to 3.3-V logic. Going to 3.3 V saves power in the drive's digital circuitry, although most manufacturers already employ low-power CMOS components. But it's the motor that consumes the most power, so moving to 3.3 V won't result in much of a power savings. For motors, the reduced voltage simply means that a higher current would have to be applied, negating any power savings.

More current is needed because a motor's torque (expressed in oz.-in.) per ampere of current, usually known as KT, is fixed. Insufficient current at a lower voltage of 3.3 V means a longer motor spin-up time, thus lengthening the disk-drive response time. In addition, if the motor takes longer to spin up, the electronics must be kept awake for an extended time, and that drains the battery faster. It's also important to maintain a consistent motor velocity or rpm, since the drive ICs are designed to work at a specific velocity and are tuned for a particular signal amplitude from the head.

PCMCIA STANDARDS

The PCMCIA standardization issue of moving to 3.3 V also must be considered. If a PCMCIA-based drive was designed to run at 3.3 V, plugging it into a 5-V slot could be disastrous. The PCMCIA committee is still working on how to implement the 3.3-V cards. But because of the current flood of 5-V cards, system designers wouldn't want to alienate that large installed base. Hence, the PCMCIA committee must come up with some solution that allows either type of card to be used.

Ben Alaimo, vice president of engineering at MiniStor Peripherals, says, "We're not working on a 3.3-V design right now because people haven't really asked us for it yet. Motor-drive 3.3-V chips are available and 3.3-V read-channel ICs have started to appear over the last few months. But we haven't seen a 3.3-V CPU from our supplier (Zilog) yet."

Aside from lowering the power and raising reliability, one of the difficult aspects of building a 1.8-in.

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disk drive is reducing the height of the ICs. Also, the physical board area that's allotted is obviously smaller than previous-generation drives. One way to fit all of the electronics on the smaller board is to increase the level of IC integration (reducing the chip count) and eliminate some of the passive components. One chip that's currently under design at a major disk-drive IC manufacturer combines the DSP IC, the CPU, and the servo-function ASIC. While this will help reduce the drive's overall size, it shouldn't affect performance. A performance boost will come when the IC manufacturers improve the interface between the CPU and the digital-signal processor.

Some of the drive's components could be moved to the system's motherboard, but several firmware issues would have to be resolved. For example, will the power management be handled by the drive's CPU or the host processor? In addition, the drive wouldn't be a standard product that anyone could simply plug into any system. It also would require much more coordination between the drive and system manufacturers.

Although many drive and system makers claim complete PCMCIA compatibility, that just isn't the case yet. Says Alaimo, "Every system has its unique quirks. For example, one system may be noisier than another due to a noisy power supply. Or, because there are some undefined pins on the connector, a drive manufacturer might try to add a feature that causes an incompatibility with some systems."

No extra ICs are needed to implement a PCMCIA interface. The interface chip is basically an IDE chip with a modified bus interface. Many drive designers have opted to keep the drive sequence the same for both PCMCIA and IDE interfaces to simplify the design. A few extra commands are required to implement the PCMCIA interface in the firmware. □

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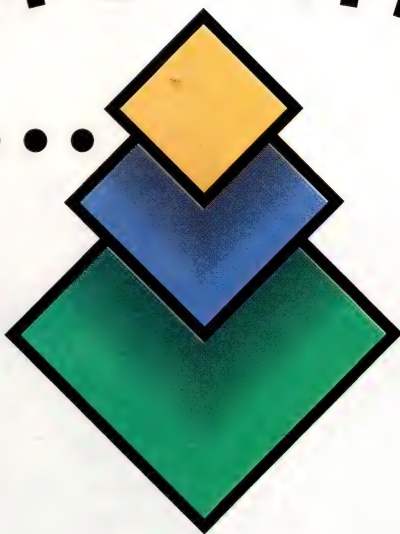
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Total # of Gates	330	2,000	660	2,000	4,000	6,000	10,000	14,000	18,000	22,000	32,000
# Usable Gates	270	1,800	600	1,800	3,600	5,400	9,000	12,600	16,200	19,200	28,800
Commonly Used Packages	16SOIC	20SOIC	44PLCC	68PLCC	84PLCC	100PQFP	128PQFP	144PQFP	160PQFP	160PQFP	208PQFP
	14SOIC	16SOIC	28PLCC	44PLCC	68PLCC	84PLCC	100PQFP	100PQFP	144PQFP	144PQFP	160PQFP
		14SOIC	20SOIC	28PLCC	44PLCC	68PLCC	84PLCC	84PLCC	100PQFP	100PQFP	144PQFP
			16SOIC	20SOIC	28PLCC	44PLCC	68PLCC	68PLCC	84PLCC	84PLCC	100PQFP
							44PLCC	44PLCC	68PLCC	68PLCC	84PLCC
									44PLCC	44PLCC	68PLCC

The above table is a sampling of available packages.

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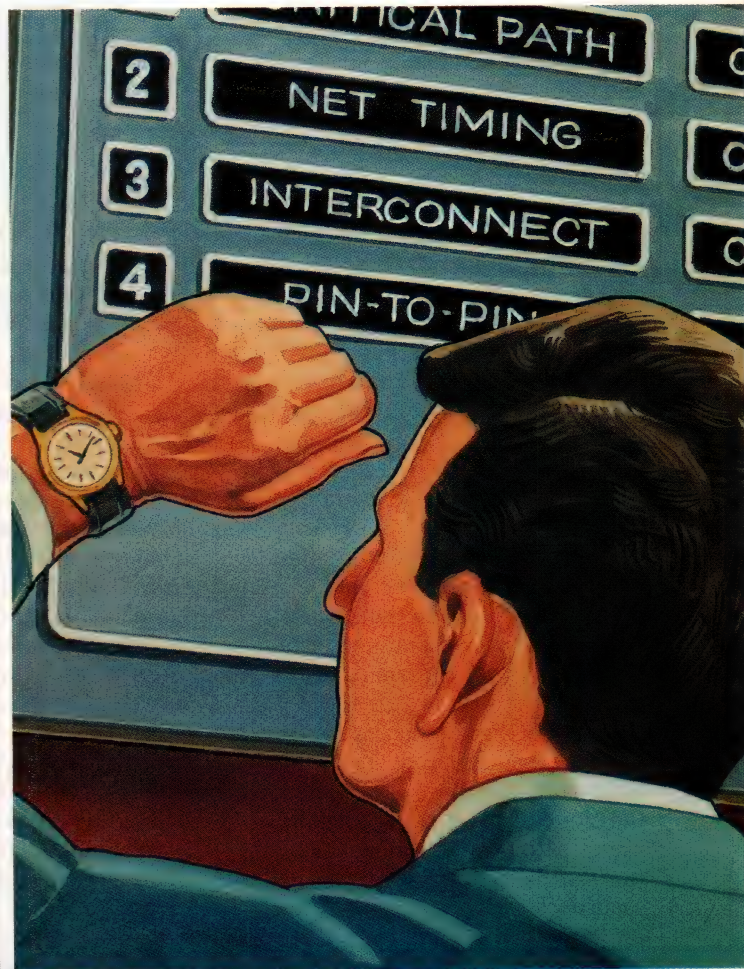
SUBMICRON ASIC TOOLS ENHANCE PREDICTABILITY

LISA MALINIAK

Multilayer-metal submicron ASIC technologies, which produce smaller die sizes and faster circuits, come with obvious cost and performance benefits. Submicron ASICs that provide 600,000 usable gates could allow engineers to squeeze an entire system onto one chip. On the other hand, the smaller geometries that make such densities possible also make timing-delay predictions and routing within die-size constraints much more difficult. While design tools in both the logical and physical domains exist for such ASICs, the lack of accurate timing models and a failure to establish tight bidirectional links have stood between engineers and first-silicon success for their submicron ASICs.

Building an environment that improves productivity and minimizes risk in submicron design is no small task. But LSI Logic and Synopsys, through an alliance that combined and enhanced their physical and logical tools, can now give engineers a new design flow that specifically resolves the problems associated with submicron ASICs. For instance, a nonlinear delay model smooths the way to predictable design. Moreover, routability was improved and design-for-test capabilities added, with enhancements made to the synthesis libraries to support those developments. The progress fostered by this alliance is significant to the entire design community because it can eventually be extended to submicron ASIC technology from other vendors.

Two types of tools are required to put a complete system on a chip with minimal design risks. As a result of design complexity and critical time-to-market pressures, high-



level design-automation (HLDA) tools are needed to create and verify designs at an architectural level, and then automatically translate, or synthesize, the architectural descriptions to the gate level. Second, engineers must have silicon-specific tools to implement their designs in the target ASIC technology.

Existing tools from LSI Logic and Synopsys provide these two critical elements of a total ASIC design environment. For its part,

SUBMICRON ASIC DESIGN ENVIRONMENT

Synopsys provides an HLDA environment that creates architectural descriptions with the VHDL or Verilog hardware-description languages. The company's simulator verifies VHDL designs at the behavioral level. Then, Synopsys' synthesis tools automatically translate the VHDL into gate-level circuit descriptions and generate test vectors. A similar flow works with the Verilog language.

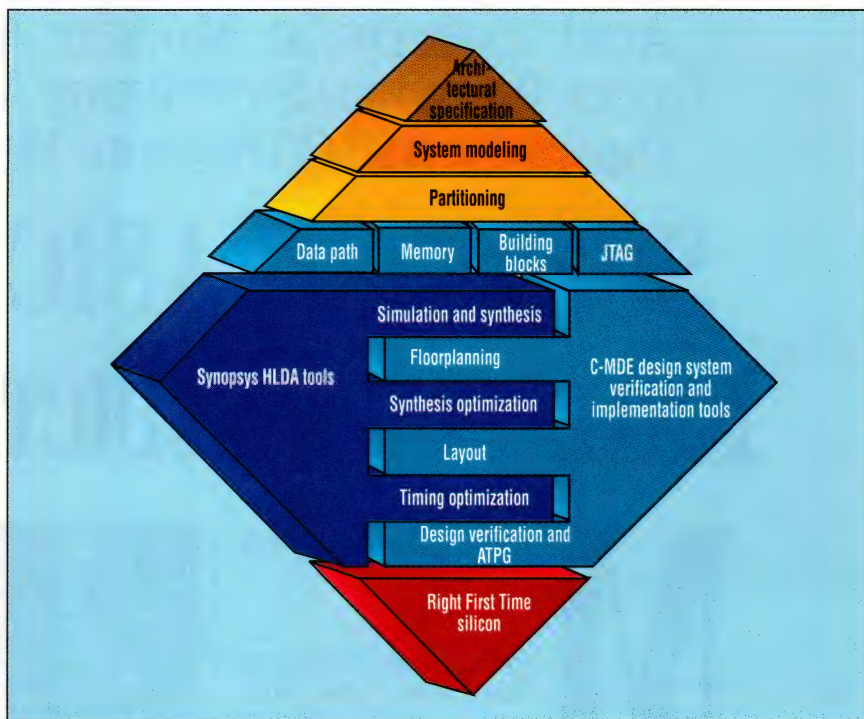
On the physical side, LSI Logic's Concurrent Modular Design Environment (C-MDE) software is a silicon-specific ASIC-design environment that transforms gate-level descriptions into working ICs. The key tools here perform floorplanning, place-and-route, design verification, and test analysis.

In each of these environments, engineers can move freely from tool to tool. However, the interface between the two is essentially a one-way path. Some design data can be fed back from C-MDE to the Synopsys synthesizer, but for submicron designs, the feedback loop is inadequate. The tricky timing involved in submicron design dictates that more back-end physical information than was required for larger geometries be made available to the front-end synthesis tools to create working silicon.

The new design flow created by the two companies minimizes engineers' risks while maximizing design throughput and circuit performance (Fig. 1). Layout information can be fed easily from the LSI Logic environment to the synthesis tool. With a bidirectional communications path, timing constraints can move from the synthesis tool to layout, and the physical implementation information can be passed from the layout tools back up to synthesis.

SUBMICRON MODELING

Links between the environments improve the design flow, but it's also critical to have submicron models that more accurately predict circuit performance early on. The two companies had to develop a modeling and delay-prediction approach in all Synopsys tools that accurately predicts the delay characteristics of LSI Logic circuits.



1. THE OVERALL submicron-ASIC design flow starts at the architectural specification, and works down through synthesis and physical design to first-time-success silicon. The Synopsys HLDA software and LSI Logic C-MDE tools are tightly meshed through synthesis-to-layout links.

LSI Logic's tool designers realized that delay modeling must rely on nonlinear equations for the smaller geometries. Making that shift would help close the predictability gap. Another step toward predictability was to bring the Synopsys tools' modeling in line with this thinking. Up to this point, the results produced by the two companies' tools began to diverge in terms of timing closure as designs moved from synthesis to the physical domain.

With this shift from linear to nonlinear modeling, the two companies took a significant step toward ensuring that the modeling corresponded in the logical and physical realms. According to LSI Logic, engineers in the Synopsys environment who use the nonlinear models can predict timing to within 5% of the C-MDE results. So even before layout, the models correspond very closely.

The Synopsys nonlinear delay modeling closely approximates submicron silicon behavior. It's based on output load plus input transition time, and maintains run-time performance during synthesis. As a bonus, the existing Synopsys static-timing

analyzer supports this nonlinear cell-delay modeling.

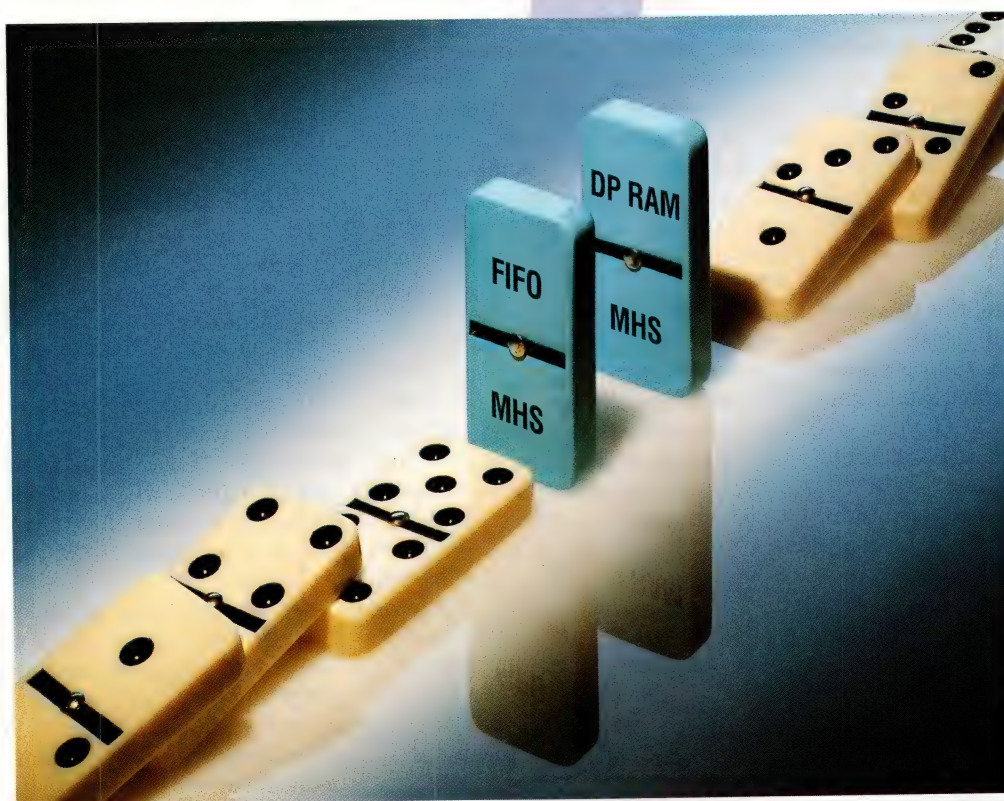
On the other hand, LSI Logic's nonlinear delay modeling is based on input ramp time as a function of output load, plus input switching threshold. The model has three major parameters: a piece-wise linear-delay equation mapped against capacitive loading, the input ramp time of each cell determined by the previous stage, and the input switching threshold of each cell defined by circuit design. As stated, the timing correlation between the two companies' models is within 5%.

After ironing out the modeling problems, the next step in improving timing predictability was the linking of high-level design to physical design. For instance, the new models help show the circuit's timing behavior. But links to layout are needed to help determine the actual length of the wires.

The challenge in linking high-level and physical design of submicron circuits is to make two very different, yet interdependent, processes work together efficiently. LSI Logic and Synopsys address this problem with

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SUBMICRON ASIC DESIGN ENVIRONMENT

several stages of product offerings, each of which move engineers closer to predictability between synthesis and physical design. This, in turn, reduces the costly repetitious cycles of design iterations.

Enhancements in the first stage of product offerings bring back-annotation data from layout into the synthesis environment. The primary benefit of this is that once the Synopsys tools are armed with the post-layout data, they can use this more accurate timing data to reoptimize a design and correct violations. Such first-stage enhancements work with LSI Logic's design kits for C-MDE version 2.1.

In the second stage, the two companies go further to closely integrate synthesis and timing-driven layout. By driving constraints forward from synthesis into layout, engineers will see a more predictable physical implementation.

Timing-driven layout, which aims to build circuits that are correct by construction, requires control of timing during physical design. This control is implemented by means of timing constraints that are set up in the synthesis tool so that the tool can identify critical paths. Synopsys passes this data in the form of a Stan-

dard Delay Format (SDF) file, allowing the layout tool to produce nets matching the constraints (*Fig. 2*). These enhancements are found in version 2.2 of LSI Logic's C-MDE design system.

Another key element in improving timing predictions is post-layout optimization. This technique is used when a design doesn't meet timing constraints after layout. Synopsys developed In-Place Optimization (IPO), a process that exchanges cells of different drive strengths along the critical path to improve timing performance. By swapping cells of identical functionality but different drive strength, IPO resolves critical-path issues without requiring another complete layout and iteration of synthesis and optimization. After IPO modifies the net list, the incremental changes are merged back into the physical design representation by a floorplanner or layout tool. LSI Logic offers a merge capability to automate this process.

For the IPO process to succeed, the lumped capacitance and pin-to-pin delays on each net within a circuit must be back-annotated from the floorplanner or layout tools by means of SDF files. Then, the IPO process can update delays as it

swaps in higher- or lower-drive cells to optimize a given critical path. This tweaking is to within $\pm 10\%$.

Until Synopsys' IPO became available, engineers were forced to recompile whole sections of the design to meet timing constraints. But doing so had a tendency to create a synthesis-layout loop that doesn't converge. Now engineers can make incremental changes that they patch into the layout through an engineering change order (ECO).

FLOORPLAN MANAGEMENT

In submicron geometries, increased resistance and capacitance dominate the delay calculation. In fact, LSI Logic found that wire metallization in its 0.6- μm , three-layer-metal ASICs contributes about 60% of the path delay. The gate delays associated with larger geometries were more linear than these wire-loading effects, which now become a first-order effect rather than the second- or third-order effect they were previously.

Because linear delay models don't produce reliable results for these conditions, engineers had problems predicting how a chip would perform when it was built. As a result, design-cycle times grew because more iterations between front- and back-end tools were needed to work out timing and other design kinks.

Currently, the two companies are working on the third stage of enhancements embodied in a new technology called floorplan management. The idea is to move physical design forward by actually bringing physical data into the design-creation process. The anticipated benefits are to reduce the number of design iterations while also squeezing out more performance.

Synopsys' Floorplan Manager tool works with LSI Logic's existing floorplanner to bring estimated net-delay information into the synthesis process for use during a circuit's timing optimization. With Floorplan Manager, engineers can simultaneously manage logical- and physical-design hierarchies.

After floorplanning in the C-MDE environment, Floorplan Manager reads timing, parasitics, and the designs' physical hierarchy. With this

AN OVERVIEW OF PDEF

The Physical Design Exchange Format (PDEF), developed by Synopsys with the cooperation of several semiconductor vendors, provides a standard medium to pass physical-design information between high-level tools and other design software. For instance, it can be used to back-annotate physical-design information from floorplanning and layout to those tools in the front end. It also can communicate physical constraints from front-end synthesis, timing analysis, and partitioning to the back-end implementation software. Synopsys intends to evolve PDEF into a standard.

The current format defines a standard set of attributes describing particular types of physical information, and can easily be ex-

tended to capture more when needed. It wasn't necessary that PDEF contain net-list information, because standard net-list formats like EDIF and VHDL already exist. Similarly, it doesn't contain any delay data, as there are now several standardization efforts going on in that area.

PDEF captures an abstract view of physical design, and is centered around the idea that the various stages of implementation with which a high-level tool might interface are all based on cell clustering. However, there's certainly more to physical design than just clustering cells. Synopsys wants PDEF to be a means of communication between front-end and back-end tools. Such a flow occurs in every design, yet there currently is no standard.

SUBMICRON ASIC DESIGN ENVIRONMENT

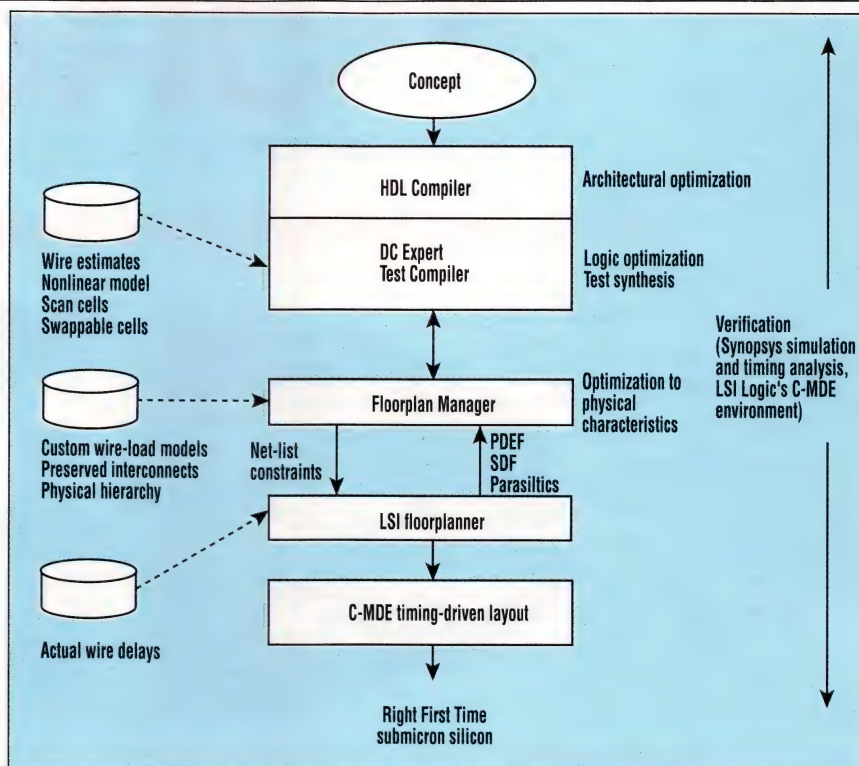
information, Floorplan Manager calculates accurate interconnect delays by building custom net models within physical clusters, while preserving delays between clusters. Engineers can then resynthesize their design based on its physical characteristics. The Floorplan Manager makes fundamental trade-offs in terms of logic timing, splitting off of logic paths, architecture, and more. Without the clustering information provided by the tight link to the LSI Logic floorplanner, synthesis can't perform these tasks.

The information exchange that enables floorplan management is made possible by the Physical Design Exchange Format (PDEF) developed by Synopsys (see "An overview of PDEF," p. 64). Floorplan Manager reads and writes PDEF files to interface with various floorplanning tools. LSI Logic's C-MDE environment uses PDEF to feed the physical hierarchy up to Floorplan Manager so it can create more smaller, more statistically accurate wire-load models (Fig. 2, again). This step was enabled by the development of PDEF. Now Synopsys' tools can perform full or incremental synthesis based on the physical-design information.

Another main area of concern for synthesized submicron designs is routability, a problem that the companies worked on together. Certain cells are more routable than others because they can route through their feedthrough channels. But if a design calls for extensive use of other cells, routing blockages may occur.

Synopsys incorporated a new constraint category in its synthesis tool that lets engineers trade off routability for timing and area. LSI Logic and Synopsys teamed to measure the feedthrough area versus the entire area of a given cell. That data was inserted into the LSI Logic libraries so that the synthesis tool knows which cells to choose based on the engineer's trade-off options.

The data supplementing the cell library includes the wire area that results from routing. This information enables synthesis to consider wire area, as well as cell area, when trading performance versus area. Previously, the area estimation was artificially optimistic. The net effect of the



2. RELIABLE INFORMATION exchange is the key to linking front- and back-end design that yields predictable results. The industry-standard SDF allows C-MDE timing-driven layout to back-annotate accurate timing data up to the Synopsys synthesis software. Also, PDEF enables LSI Logic's floorplanner to pass important physical information to the Floorplan Manager. This data exchange spreads verification across the entire design cycle to produce a circuit that works.

enhanced library is that predicted area will be closer to reality, allowing engineers to optimize and improve wire area by up to 10%.

TESTABILITY

As the number of gates per pin grows with the advent of submicron ASICs, the need for design-for-test with synthesis becomes more pressing. Design-for-test with synthesis means incorporating testability analysis during the first synthesis pass. LSI Logic and Synopsys joined forces to define test vectors so that the Synopsys Test Compiler tool provides automatic test-pattern generation in LSI Logic's format. In addition, LSI Logic added scan cells to its Synopsys library as well as a greater variety of scan styles for use with the Test Compiler software.

Finally, other enhancements were made to LSI Logic's Synopsys-synthesis libraries, including the company's 300K and 100K gate-array, embedded-array, and cell-based librar-

ies. LSI Logic's 300K CMOS technology has a 0.6- μ m gate length, a 0.45- μ m channel length, a choice of two or three metal layers, and 600,000 usable gates. The 100K CMOS technology features 1.0- μ m drawn gate length, 0.7- μ m channel length, two layers of metal, and 100,000 usable gates. The 500K libraries will be enhanced for release in the third quarter of 1994. They consist of a 3.0-V CMOS technology with 0.5- μ m gate length, 0.35- μ m channel length, four layers of metal, and a 1.5-million-gate capacity.

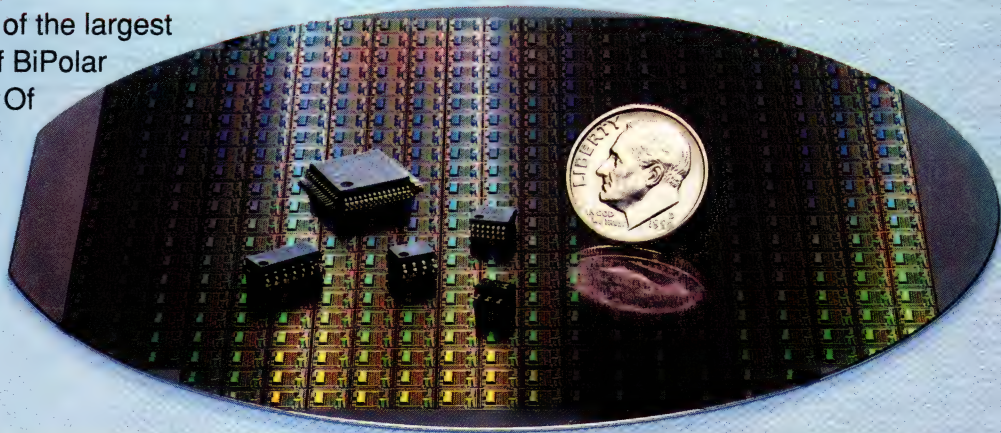
The actual library enhancements include improved wire-load models that feature additional area and resistance data. These models enable the Synopsys synthesis tool to better estimate the effects and costs of interconnections. Also, there are now additional wire-load models for three-layer metal. These are separate from two-layer-metal wire-load models. An on-line documentation feature offers guidelines for using

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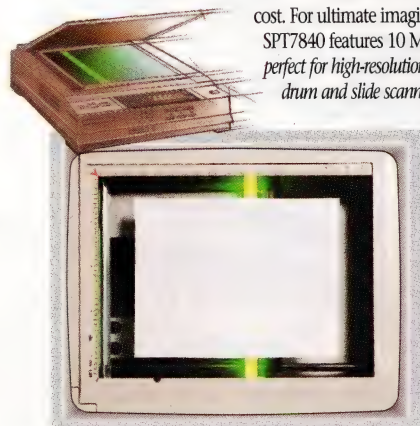
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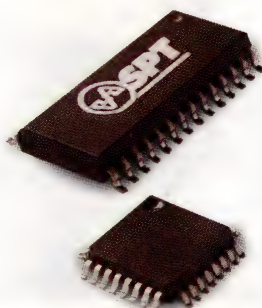
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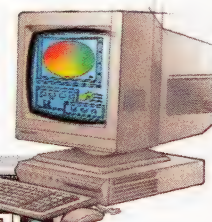
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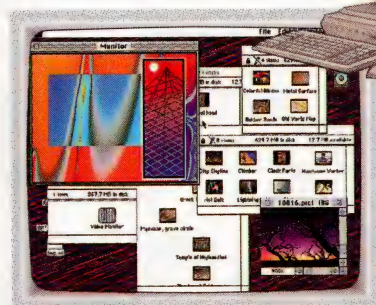
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SUBMICRON ASIC DESIGN ENVIRONMENT

Synopsys Synthesis Libraries.

In the future, Synopsys and LSI Logic will work to further ease the design of submicron ASICs. The original alliance, announced in February 1993, called for ten years of joint development and marketing. Projects underway include the creation of VITAL-compliant sign-off quality libraries for the Synopsys VSS simulator. This will improve predictability and time-to-market by eliminating the need to switch to a separate set of sign-off tools to achieve LSI Logic Right First Time silicon. In addition, this work is necessary to attain design hand-off earlier in the design cycle at higher levels of abstraction.

Other work is being done to improve synthesis libraries and more efficiently incorporate design reuse. For optimal silicon designs from the Synopsys synthesis tool, LSI Logic will continue experiments to deliver the optimal cell set that allows engineers to build the fastest and densest circuits possible with a particular library. And as chip capacities grow beyond 1.5 million gates, efficient design reuse becomes essential. □

PRICE AND AVAILABILITY

Floorplan Manager, which includes PDEF support, is available in Synopsys' V3.1 software release that's shipping now. The tools run on a variety of Unix workstations. Pricing for the Design Compiler, HDL Compiler, Test Compiler, and Floorplan Manager is set at \$65,000, \$20,000, \$50,000, and \$40,000, respectively.

Six of LSI Logic's synthesis-optimized libraries and C-MDE 2.2 design-verification tools began shipping this month. The following libraries are shipping now: LCA300K, LEA300K, LCB300K, LCA100K, LEA100K, and LCB100K. Three more libraries—LCA500K, LEA500K, and LCB500K—will ship during the third quarter of this year. PDEF support will be available in C-MDE 2.3, which ships in July. C-MDE runs on Sun workstations, and lists at \$45,000. The libraries are available for any platform supported by Synopsys. Pricing is set at \$5000 per library.

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MODERATELY	531
SLIGHTLY	532

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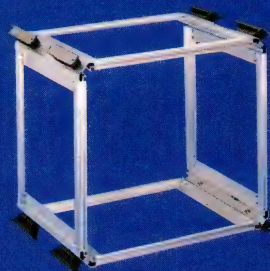
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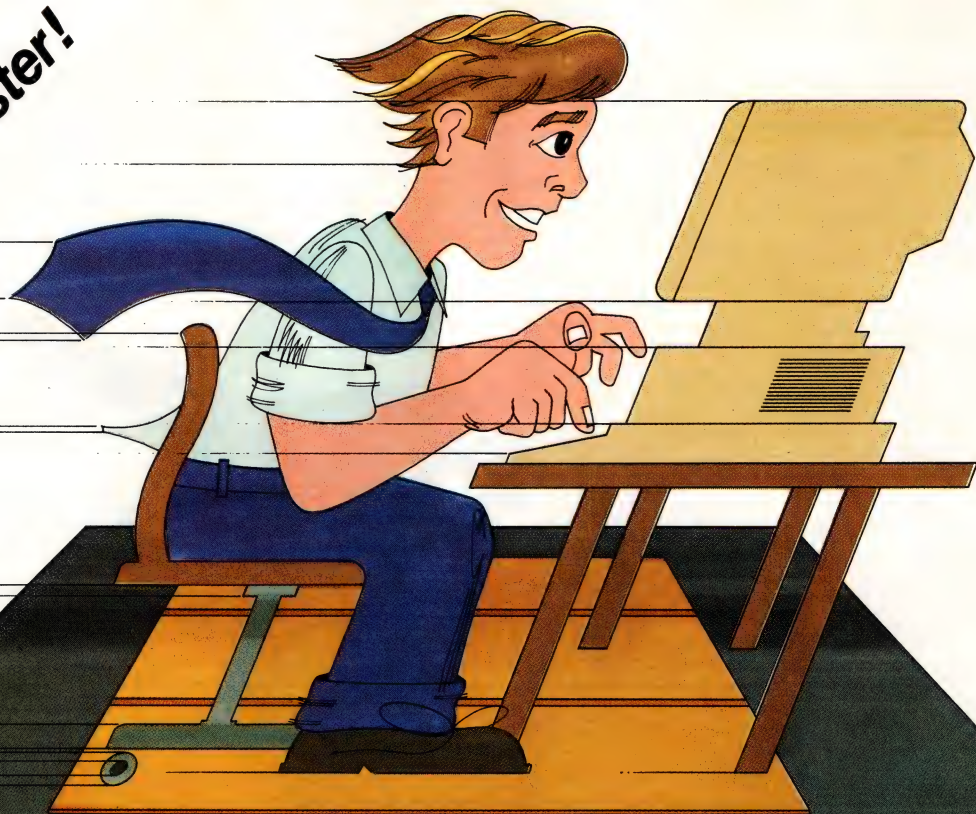
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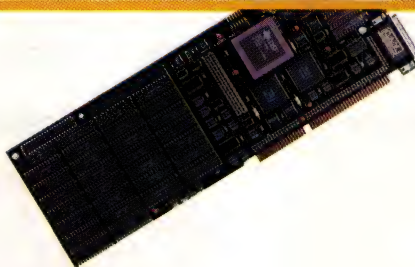
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PROCESS IMAGES FAST WITH A REAL-TIME OS

SOFTWARE BASED ON BITBLTs USES A DISPLAY LIST THAT COMBINES DRAWING INSTRUCTIONS AND COMPACT DESCRIPTIONS OF FONTS AND OTHER OBJECTS.

No longer confined to supercomputers and dedicated systems, high-powered graphics and imaging applications have moved onto desktop platforms, stepping up demands for fast CPU performance along the way. On the software side, real-time software in embedded graphics-intensive subsystems is called upon not only to output images in real time, but also to perform real-time transformations of graphics and image formats. Real-time software also must interact with high-density data sources, such as digitizers and frame grabbers.

The common thread running through most graphics and imaging subsystems is the need to acquire, store, manipulate, and output the large arrays of data that describe images. The size of the memory array and the need to drive output devices like displays or printers combine to produce real-time performance requirements. Real-time response is crucial because, for example, a person viewing an image on a monitor would view an incorrect image if the imaging subsystem can't respond to changes in real time. Likewise, a marking engine prints a page incorrectly if the imaging subsystem can't feed the data to the engine on time.

While real-time performance is key, meeting customer pricing expectations is also a requirement. And traditional design techniques don't necessarily result in the lowest-priced products. For example, the simplest way to represent an image in memory is with a bit map. One or more bits of memory describe each pixel of the image. Many graphics and imaging products use this brute-force, bit-map approach because paying the price for the large memory array may simplify other aspects of the design. Memory cost can be substantial, though. For instance, some new 600-dot/in. laser printers require 6 Mbytes of RAM to print a full-page PostScript image. At current memory prices, the RAM requirement can add \$150 or more to the printer's base price—well over 10% of the retail cost.

MINIMIZING MEMORY

To shrink product cost, designers must develop ways to minimize the size of the memory array integrated into graphics and imaging devices. Two interrelated techniques can serve to reduce the memory required. First, the subsystem design can take advantage of data/image compression tech-

STEVE BUTTERFIELD

Peerless Systems Corp., 2381 Rosecrans Ave., El Segundo, CA 90245;
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niques to reduce the amount of memory to describe an image. Second, designs can harness real-time software on fast CPUs, as well as on dedicated coprocessors in some optimum cases, to manipulate images stored in formats that require less memory than bit maps.

Graphics and images can be represented with a number of data formats that offer various advantages over a bit-map representation. Generally, the alternative formats require less storage space, allow simpler manipulation of the image, and/or provide hardware independence at one or more levels.

A simple example of a data format that represents an image, or, more exactly, a symbol within an image, is the use of ASCII codes to represent alpha-numeric characters. A computer program such as a word processor can manipulate the ASCII

codes that comprise a sentence much more easily than it could the individual bits in a bit-map representation. Of course, those ASCII codes must be converted to a bit map for display on a monitor or for output on a raster printer (e.g., a laser printer).

Common data formats used to store, represent, manipulate, or create graphics and images include:

- TIFF, PCX
- JPEG (Joint Photographic Experts Group)
- DRW, CDR, CGM
- EPS (Encapsulated PostScript)
- Windows/GDI (Graphics Device Interface)
- PostScript
- PCL (Printer Control Language)

Created for specific purposes, each of these formats offer easily recognized characteristics along with vari-

ous advantages.

TIFF and PCX formats are used as a compressed format for bit-mapped or raster images. For example, an image captured by a scanner or frame grabber and stored as a PCX or TIFF file needs much less storage space than the actual bit map. Moreover, an application such as a painting program that creates raster-type images would use a format like PCX or TIFF to store data. In fact, the formats regularly serve to move raster-type images between computers.

To reduce file size, TIFF and PCX both use variations of run-length coding, which compresses data by representing repetitious runs of a bit or bit pattern with a code. TIFF and PCX are lossless compression schemes—that is, the bit map reconstructed from a TIFF or PCX file is, bit by bit, identical to the original source. As images, particularly color

IMAGING SUBSYSTEM ARCHITECTURE MIMICS DESKTOP ENVIRONMENT

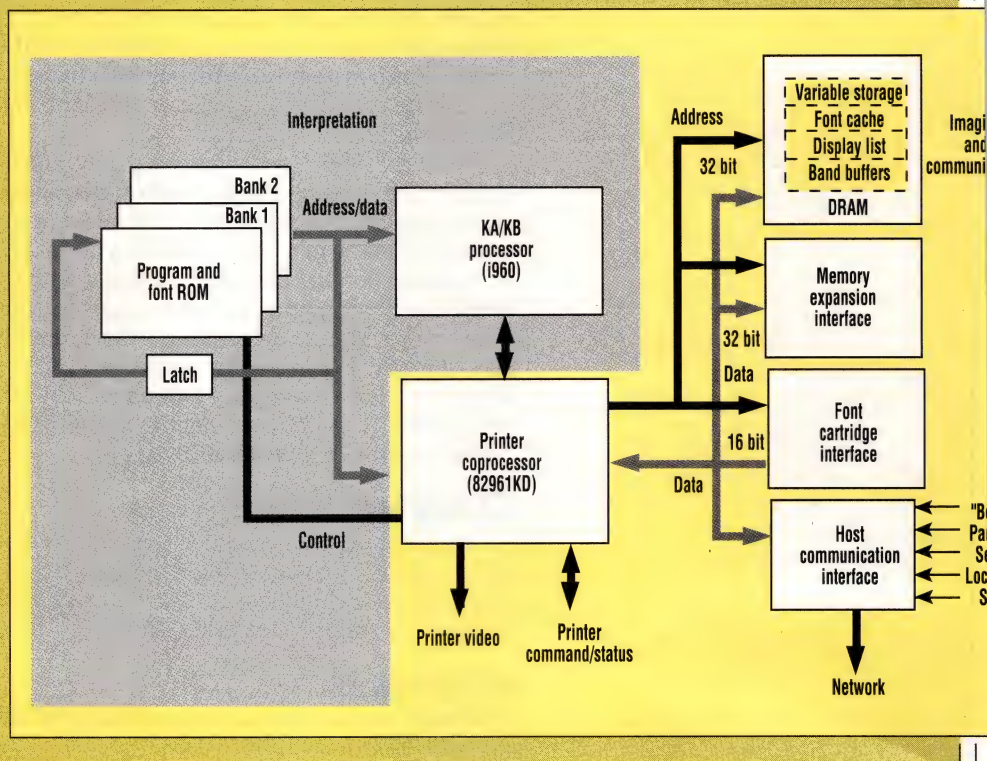
The architecture of a graphics or imaging subsystem such as a printer controller closely resembles that of a desktop computer. The subsystems include a processor, ROM, RAM, I/O, communication interfaces, and an operating system. Both are likely to use coprocessors—the desktop architecture for floating-point or graphics acceleration and the graphics subsystem for finer-grain acceleration of a specific function like a BitBLT. The graphics subsystem typically employs a multitasking real-time operating system (RTOS) as opposed to the use of DOS or Unix on the desktop.

A typical printer controller subsystem (see the figure), based on Intel's 960 RISC processor, uses Intel's 82961KD Printer Coprocessor, which combines a graphics execution unit with the memory and I/O controllers required in a printer. Motorola's design

ups integration by combining a 68000 core and a graphics processor on the 68322 IC.

The controller relies on application programs just like a desktop computer. For a controller, the application programs handle vari-

ous tasks, including PostScript interpretation and font management. Once the application program interprets a PostScript or other PDL file, the graphics coprocessor can render the image into bit-map form.



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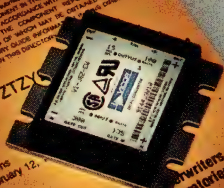
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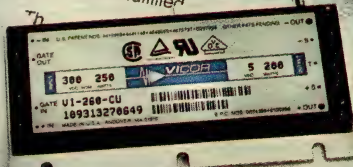
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images, approach photographic quality, lossless methods don't provide sufficient compression ratios for file storage or file transmission over data links such as dial-up modems. JPEG can be used in these cases to provide additional compression, although the compression method is lossy. The compression algorithm throws away some data, but the missing data isn't perceptually significant to the human eye.

HIGH-LEVEL FORMATS

While the raster formats are suitable and required for many imaging applications, a drawing application can manipulate data more easily when it's stored as objects described by one or more vectors or arcs. Such programs include CAD packages and business-graphics packages like Corel Draw. Formats that are used include DRW, CDR, and CGM to store data.

As image complexity rises and the images combine raster and vector data types, a higher level format is required. The higher level formats such as Windows/GDI and the PostScript and PCL page description languages (PDLs) for printers are important because they add a hardware abstraction layer to the computing environment. These formats make the software, graphics, and images independent of underlying graphics hardware.

PostScript and PCL, for example, are both printer languages that describe an image for output to a printer. The printer controller actually executes (or interprets) the command sequence just as any general-purpose computer might interpret a Basic program. PCL is the language that Hewlett-Packard developed for use in its laser printers. Created by Adobe Systems for printer applications as well, PostScript can describe graphics objects more robustly in a high-level language than does PCL.

Both PostScript and PCL fall back to rely on a bit-map representation of complex raster images that cannot be represented by high-level constructs.

PostScript has become so widely supported that EPS files now are the de facto standard for moving images between different computers. Operating systems and environments such as Windows use a similar method to isolate the application programs and images from the underlying graphics hardware. Programs must access the hardware through a set of application programming interfaces (APIs) to the GDI. The GDI is a code module called a dynamic link library (DLL) that passes the application calls to a device-specific driver. In Windows environments, the GDI accesses displays and all hard-copy output devices.

The variety of data formats cre-

ates an ongoing need for transformations between formats. For example, a PC user might create a drawing using Corel Draw. The Corel Draw application works with its CDR representation on an image. The application must use GDI calls, however, to display or print the image. Furthermore, the Windows printer driver has to convert those GDI calls to PostScript or PCL instruction files for output. The design scenario becomes even more complex as users create compound documents—for example, combining text, a vector-based drawing, and a bit-mapped image in a desktop-publishing application (Fig. 1).

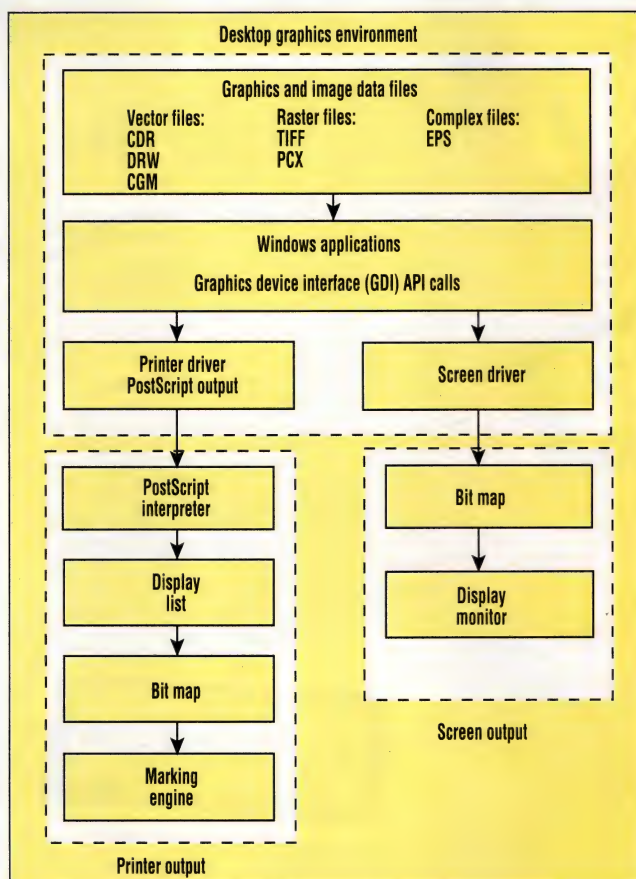
FORMAT MANIPULATION

In a desktop PC environment, these image manipulations and transformations don't typically use real-time technology. Rather, users are expected to wait patiently while the host CPU crunches the data.

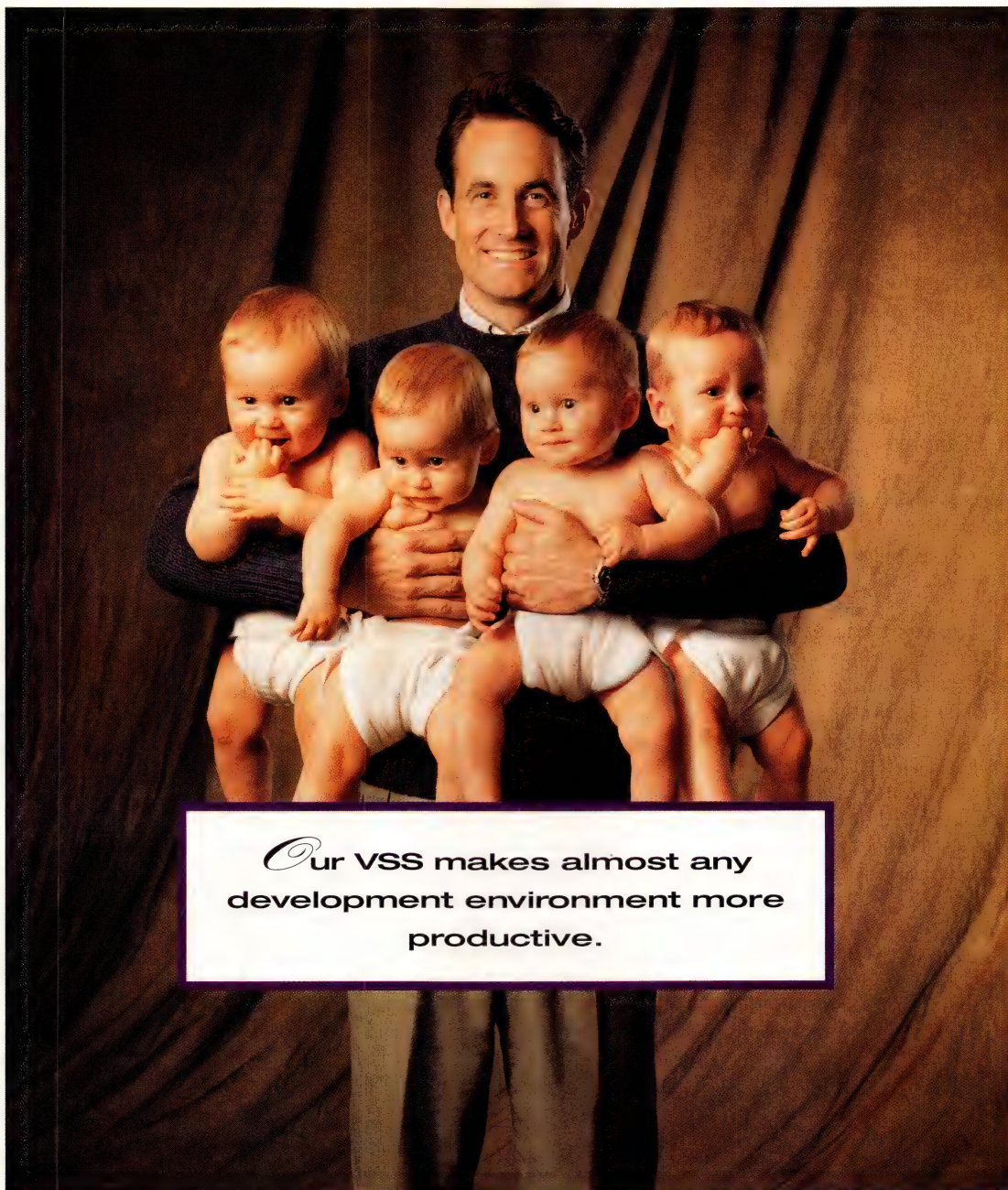
In graphics subsystems such as printers, frame grabbers, scanning subsystems, and image processors, however, any latencies in processing can result in erroneous image files. The need for real-time computing joins the need to minimize memory used in the subsystem, thereby also lowering cost.

Key to developing a memory-efficient subsystem that processes images in real time is yet another data format. Because the application program, Windows, and printer formats were conceived for specific image types and purposes, none of the formats meet the more robust requirements of a subsystem that must render, capture, and manipulate images in real time.

One way to efficiently store and manipulate images is by using a display list that can represent bit-mapped, vector- and arc-based, and text objects equally well. The display list can be tuned to provide bal-

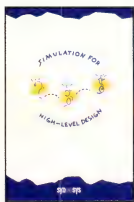


1. IN THE TYPICAL DESKTOP computing environment, graphics and image data undergoes many format transformations. Consequently, a need arises for real-time software that executes on fast microprocessors in subsystems such as a printer controller.



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ance of compression and ease of access to various components of an image. One example of a display list is the Memory Reduction technology (MRT) developed by Peerless Systems for use with its PeerlessPage real-time operating system for printing and imaging applications. To describe an image, the MRT-based software uses a display list combining drawing instructions and compact representations of fonts and other objects.

BitBLTs

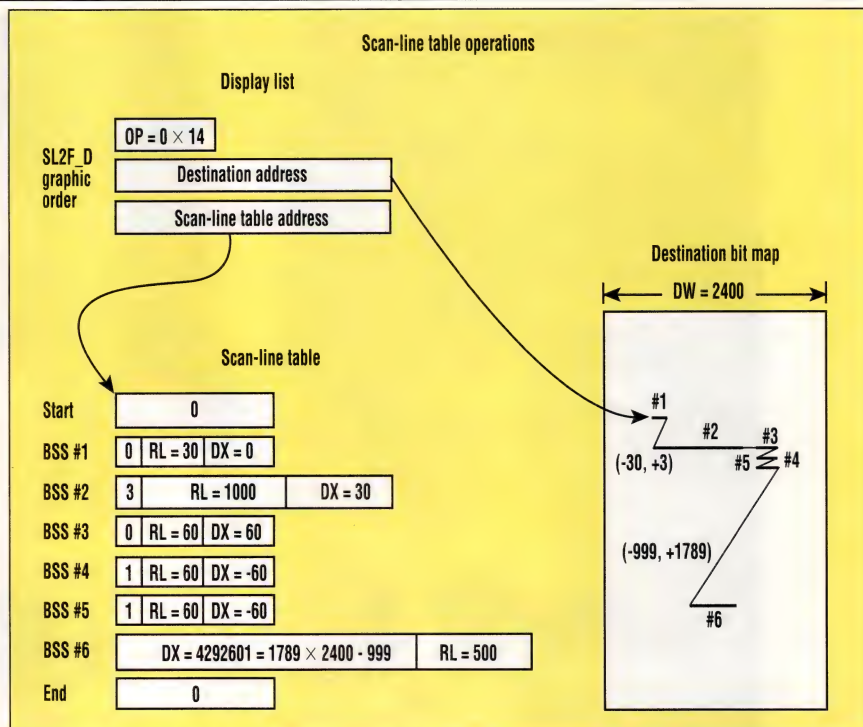
MRT technology is based on a set of graphics primitives that were designed to completely describe the graphics operations required to form an image. These primitives are unique in their ability to describe both rectangular and irregular polygonal objects.

BitBLT (bit block transfer) operations are common in all graphics devices because such devices regularly require that a block of pixels be moved from one memory location to another. For a Peerless display list, one BitBLT instruction can describe how to draw an object or move an existing bit-mapped object from one location to another. The instruction can also specify a half-tone or fill pattern simultaneously.

The efficiency of the BitBLT instructions is easily explained. For example, a bit-map representation of a one-pixel-thick line drawn across an 8.5-in. page at 300 dots/in. requires more than 300 bytes of memory. A BitBLT instruction that describes how to create the line requires less than 10 bytes. Memory savings are compounded for two-dimensional objects. For example, a single BitBLT instruction could describe a rectangular area of any size filled with a half-tone (gray) pattern.

BitBLT instructions are simple, efficient representations of almost any image component that can be described by a rectangular array of pixels. The instructions can describe most simple fonts and line art, including many graphic objects.

A display list, however, must handle all occurrences so that the format can efficiently represent more complex objects and bit maps. To describe complex objects such as irreg-

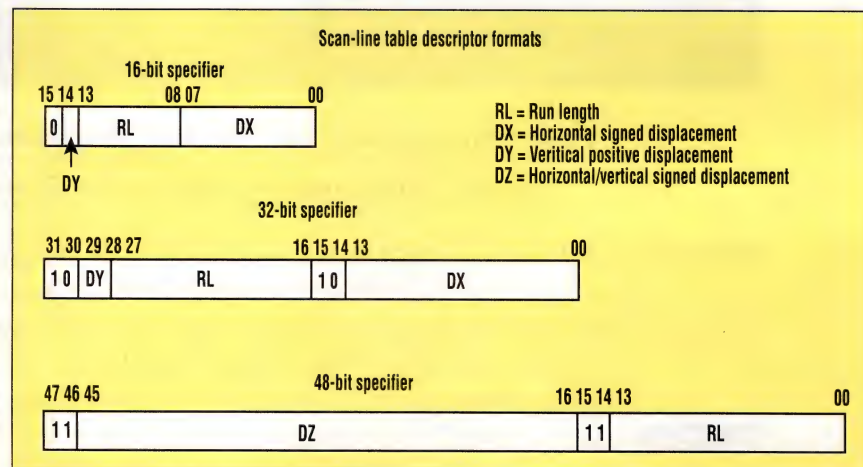


2. DISPLAY-LIST TECHNOLOGY, which forms the basis of the Memory Reduction Technology, relies on scan-line tables to compress the description of complex graphics objects and fonts. Each table entry includes a run-length-compressed description of one line segment that makes up a part of the image. Each entry also includes x- and y-axis displacements to the start of the next segment.

ular polygons and complex fonts, Peerless developed a representation called a scan-line table. The scan-line technique uses a table to describe run-length-compressed line segments that make up an image. Each entry in the table describes one line segment and includes signed displacements in the x and y dimensions that point to the destination coordi-

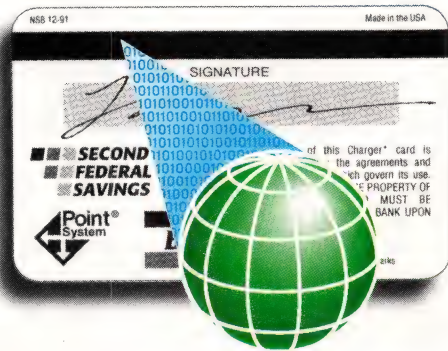
nates of the next line segment. A scan-line instruction (essentially a specialized BitBLT instruction) in the display list points to the address of the scan-line table in memory.

The scan-line table entries can take one of three formats based on the pixel displacement to the start of the next line segment (Fig. 2). The choice of 16-, 32-, or 48-bit entries is



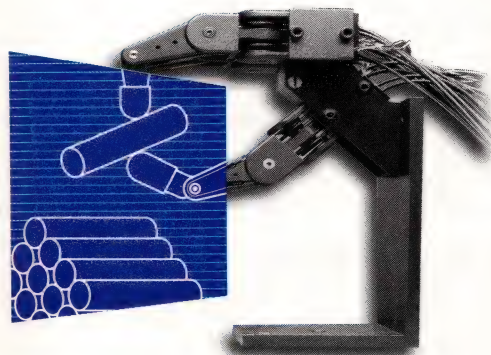
3. SCAN-LINE-TABLE ENTRIES can be 16-, 32-, or 48-bits in length, based on the length of the line segment described and the magnitude of the displacement to the next line segment.

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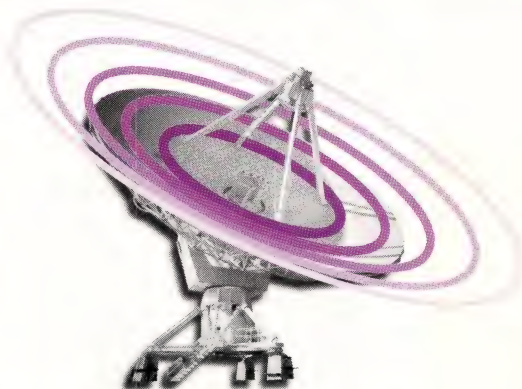
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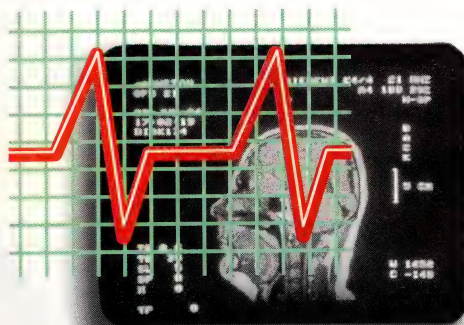
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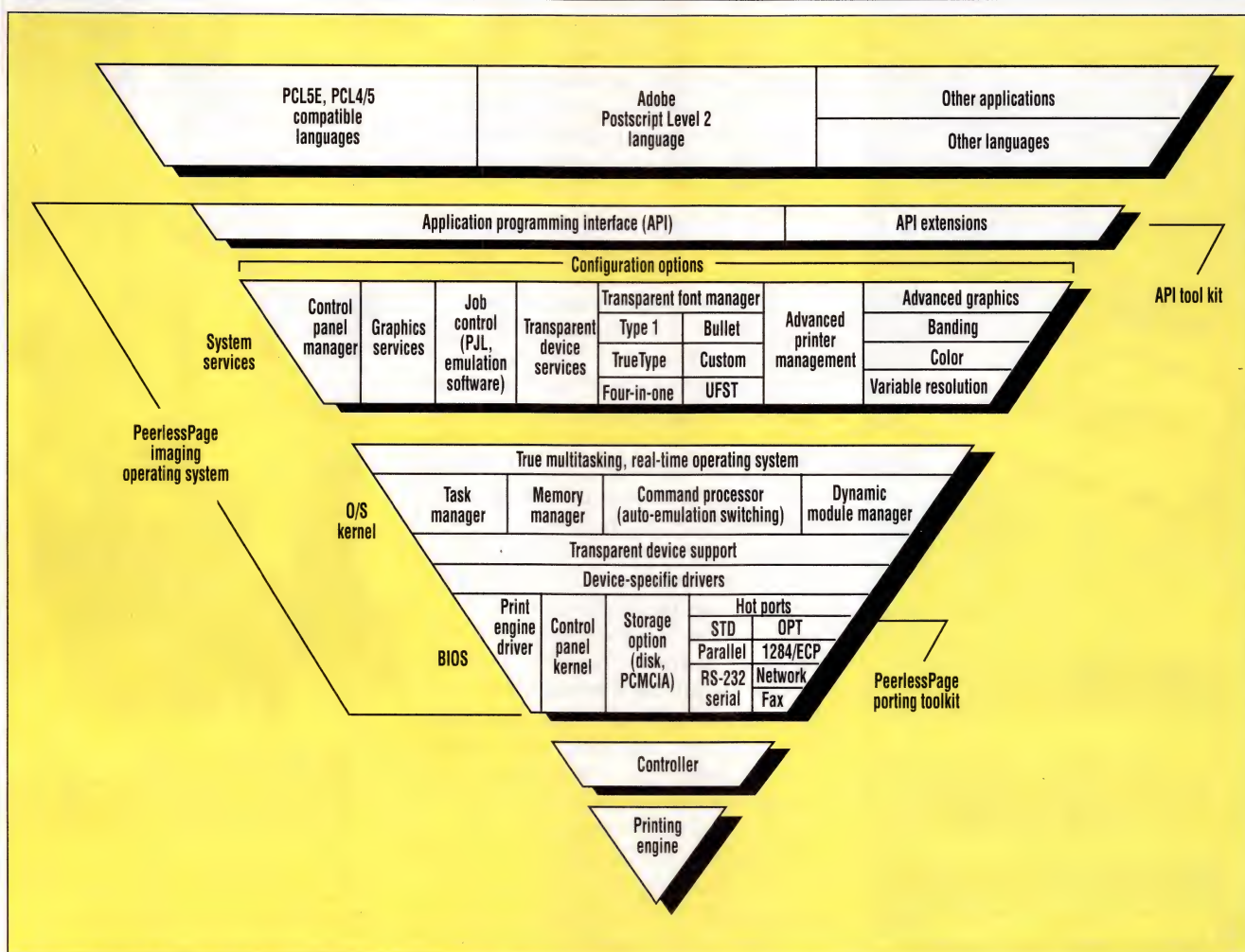
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DESIGN APPLICATIONS REAL-TIME SOFTWARE



5. A REAL-TIME operating system provides a hardware extraction layer that allows the operating system and application code to be easily ported to different microprocessor families. The PeerlessPage operating system combines a set of graphics services optimized to print and image applications with an API that has enabled porting to Intel 960, Motorola 68000, MIPS R3000, and AMD 29000 family processors.

trol rendering, and even a control panel manager. An API gives application programs access to the operating-system kernel and services.

A real-time operating system simplifies the software development task in a printing or imaging subsystem design to one of writing the application software. Some typical application programs may include a user interface, scanning, fax, image capture, and page description language (PDL).

In a printer controller, the developer must optimize the graphics rendering tasks to meet the ongoing requirement of feeding raster data to the marking engine. The code also should include error recovery mechanisms to handle Print Overrun Errors. For example, a printer may encounter a complex page of graphics that even a fast RISC processor can't

render in real time. The control task must respond in one of several ways. If the extra memory is available, the controller can render a full-page bit map before starting the marking engine. The controller also could print the image at a lower resolution to reduce memory requirements. In some cases, the controller may have to simply respond with an insufficient memory message.

Designers can build a more robust graphics handling capability into an imaging or printing subsystem by bolstering the real-time software with dedicated graphics coprocessors. For example, a graphics coprocessor can execute BitBLT operations orders of magnitude faster than the fastest RISC processors can. Using a dedicated coprocessor boosts performance dramatically and increases output quality by elim-

inating the need to fall back to lossy compression techniques when handling complex pages.

For printer applications, two such graphics processors exist (see "Imaging subsystem architecture mimics desktop environment," p. 74). Intel's 82961KD integrated printer coprocessor IC is intended for use with the 960KA/KB processor. Motorola's new 68322 processor, meanwhile, integrates a 68000 core and a graphics coprocessor on the same IC. The PeerlessPage environment includes direct support for these coprocessors, making it highly unlikely for printers equipped with the ICs to exhibit Print Overrun Errors.

A real-time subsystem that takes advantage of a coprocessor actually enables parallel processing in the subsystem—improving imaging performance with no additional memo-

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DESIGN APPLICATIONS

REAL-TIME SOFTWARE

ry. The main CPU can execute the I/O, control, and PDL applications under the real-time operating system, and the coprocessor can simultaneously manipulate and render display lists that are created by the main CPU.

While today's real-time technology is limited to specialized graphics subsystems in the desktop environment, tomorrow promises a closer integration of the technology into the desktop. Enabled by lower-cost coprocessors and more robust real-time operating systems, the changes will be required by an increased reliance on color scanning and graphics, color photographic-quality images, and even full-motion video.

The first evidence of the transition is already here. Today, printing subsystems can be integrated more directly into a Windows environment using the native GDI interface rather than requiring a translation to a PDL like PostScript. For example, PeerlessPage can host GDI print drivers. Soon the subsystems that handle display and hard-copy output may be combined completely.

Furthermore, the dropping price of color marking engines is making color printers increasingly popular. Because color typically multiplies memory requirements for image storage four- to twenty-four times, the use of an efficient display list and MRT technology will become mandatory rather than optional. Furthermore, the real-time requirements will intensify as the image size increases, because subsystems such as printer controllers will process display lists in smaller, more granular bands. □

Steve Butterfield, vice president of hardware development and co-founder of Peerless Systems Corp., currently directs hardware development activities, including the development of printer coprocessor ICs offered by semiconductor partners Intel and Motorola.

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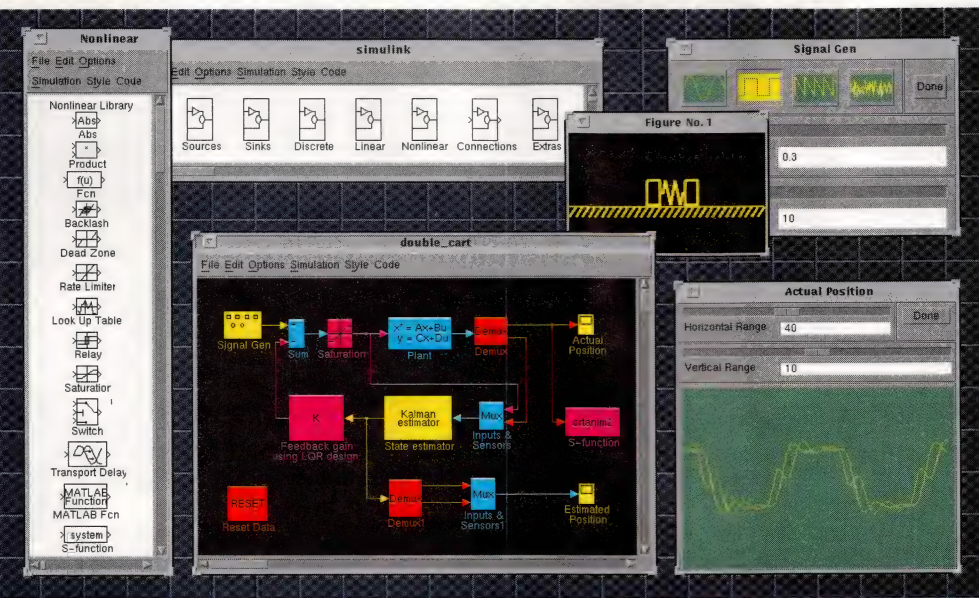
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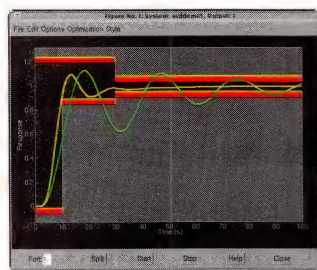
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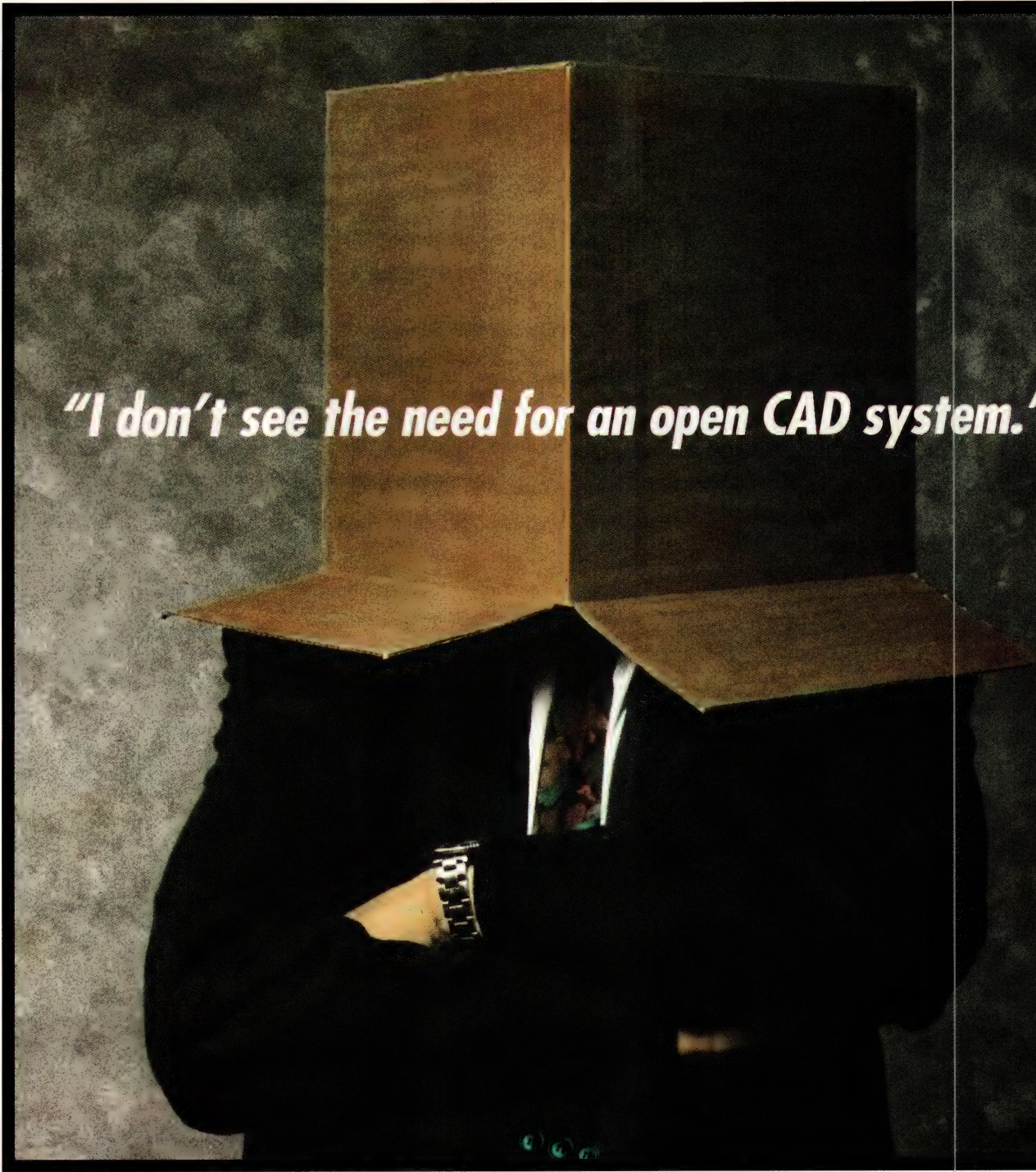
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**TAKING STEPS
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WITH
MARKETING
WILL HELP
ENGINEERS
DESIGN MORE
SUCCESSFUL
PRODUCTS.**

DONALD STEWART

Concurrency Group, 318 Bear Hill Rd.,
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T

he most enduring organizational wall in the electronics industry is the one between engineering and marketing. Each side wants what the other can't provide: Engineering looks to marketing for a crystal-clear view of customers' desires; marketing wants the perfect product.

To dismantle this wall, engineering and marketing obviously must work at improving their relationship. As a start, you can forge a stronger human link. Major improvements are possible if each function accepts its responsibility for change (it's futile to expect the other side to make all of the changes), adjusts expectations so less than perfect market clarity and products are the goals, and tries to walk in the other person's shoes to understand the limits of professional practice.

You also must work on the substance—what you discuss and how you discuss it. The reason is clear. If you view product development as a series of interlocking, close-call decisions, then the data you use and how you use it can make a huge difference in the outcome. One set of data and one way of thinking can lead to a me-too product. A different way of thinking (often with different data) can develop into an innovative and exciting product.

Closer to home, there are three reasons engineering has a strong self-interest in understanding and taking part in marketing decisions. First, marketing decisions made early in the project impact the design of the product, including features, price, manufacturability, and ease-of-support. With 80% of the product's cost and features decided before detailed engineering begins, it's important that engineering take an active role at the earliest stages of product development, including the marketing decisions.

Second, if you employ concurrent-engineering techniques, engineering should actively participate with marketing, manufacturing, and support during all phases of development.

Third, by being involved in the early marketing decisions, designers develop a stronger sense of ownership of the new product. If the product has problems, engineering will be motivated to solve them; if it meets its goals, the designers will likely continue to improve it.

This article will help you decide what to discuss with marketing and how to discuss it. With the information provided, you can assess how you currently talk with marketing and evaluate methods that could be an improvement.

CHOOSING A METHOD

There are at least six ways of discussing new products with marketing (*Table 1*). You're probably already using one of them or an in-house variation of one. You must decide if it's the best method for your needs, and if not, pinpoint a more suitable option.

A good way to choose the best method of discussing new products is to evaluate alternatives with a set of comparison yardsticks. Each yardstick measures what you discuss and how you discuss it from a different perspective. The seven yardsticks form a summary graph, with five levels between the two extremes (*Table 2*). After you've checked off the appropriate level for each yardstick, the resulting "footprint" offers useful insights into

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whether a particular method is right for your product and company. Also, the development team can compare several footprints to evaluate alternative methods.

For example, the first yardstick measures whether you use a checklist or a matrix to collect and analyze information. The difference is important. A checklist is a reminder of items to consider. It helps you answer the question, "Have we collected and considered all of the relevant data?" The limitation of a checklist is its single perspective. Most checklists ask questions from one point-of-view, such as user, repair person, distributor, or developer.

A matrix is also a reminder of items to consider, but it allows you to assess data from two or more axes, with each axis providing a point of view. For example, the matrix known as Quality Function Deployment (QFD) or House of Quality shows product attributes like accuracy and speed from the viewpoint of the customer on one axis and from a technical viewpoint on the other.

When using a matrix and its two perspectives, you're likely to uncov-

er inconsistencies, missing information, or patterns of data that would go undetected with a checklist. By employing a matrix method for product definition, you can learn important information early in the project, rather than later—maybe too late—in development.

The following is an explanation of the seven yardsticks and how the footprint should be filled out. The examples refer to a footprint for an ad hoc method of dialogue between engineering and marketing, which is the type used at more than 80% of companies (Table 3). The footprint came from a company making electro-optic systems, but if you utilize an ad hoc method, you will likely find many similarities between this example and your method.

• **Checklist format—Matrix format.** Mark column 1 if the list of items to consider is informal, undocumented, or from a single perspective. Mark columns 2 or 3 if the list is formal or documented, or if more perspectives are added. Mark column 3 for casual use of a matrix or a matrix with a few items on each axis. Mark columns 4 or 5 for formal use of a matrix and

more items on each axis.

Example: Marked in column 1 because the checklist was developed on-the-fly during discussions with marketing. The checklist is primarily from the user's perspective.

• **Less structure—More structure.** Mark column 1 if planning tools don't exist or are used casually, and if there's little or no common terminology for product development. Mark columns 2, 3, or 4 for progressively more structure. Mark column 5 if formal methods exist for project planning, and there's common terminology for product development.

Example: Once again marked in column 1 because the project was planned on-the-fly. The methods used are different, but not necessarily better, than prior projects. No standard terminology exists.

• **Technology-oriented—Customer-oriented.** Mark column 1 if the perceived value of the product is its technology and that is the claim made to customers for the product. Mark columns 2, 3, or 4 as the customers' view becomes more important in the discussion. Mark column 5 if the customers' view dominates the dialogue

TABLE 1: SOME TYPES OF ENGINEERING-MARKETING DIALOGUE

Method	Description	Pros	Cons
Ad hoc	• Uses methods at hand, especially ones from successful projects	• Learn from past successes	• No formal structure so easy to overlook essential items • Discussion often lacks depth of analysis
\$Appeals	• Takes a whole-product approach • Primarily an analysis tool	• Has a strong customer viewpoint • Useful for predicting product success in market	• Details of technology left unstructured for team • Lacks a matrix approach
Quality Function Deployment	• Formal method of product decomposition into technical requirements and market demands • Focuses attention on details of technology and markets	• Formal method • Matrix approach helps to uncover oversights/conflicts • Provides direct link to manufacturing/business processes through follow-on matrices	• In practice, favors technology over markets because more details usually known about technology • Most useful for incremental products • Easy to make overly complex • Little emphasis on intangible product aspects like customer motivation
Product Value Matrix	• Matrix method of documenting customer value • Qualitative-only data based on how the customer interacts with the product	• Focuses on customer-to-product interactions to capture less tangible aspects of product (like cognitive demands from customer and the emotions of ownership), which are considered design opportunities. • Uses matrix from the point of view of the customer	• Details of technology left unstructured for team
Crossing the Chasm	• Provides a logical chain of analysis to decide positioning for a complete product	• Tries to understand the emotions of typical users with vignettes to illustrate a product's use and the customers' thought processes. • Focuses on the complete product, not just the physical product • Includes user needs and details of technology	• Requires a facilitator to keep the analysis on track • Prompting questions are open-ended and subject to wide interpretation • May or may not use matrices
Market-Driven Business Segmentation	• Focuses on specific customers in target markets	• Uses quantitative methods like surveys to identify multiple needs of customers • Evaluates segments individually • Attempts to capture both tangible and intangible purchase factors	• No focus on technology used • Generally weak on matrix methods

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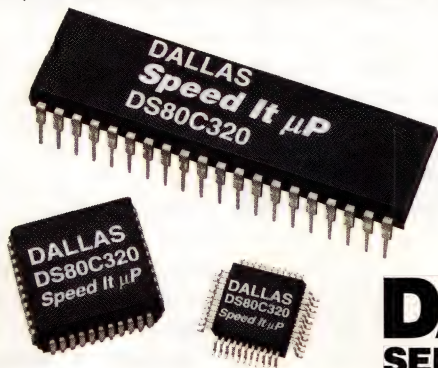
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and technology is seen as a means to an end.

Example: Marked in column 2 because most of the product's value was perceived to be its electro-optic assemblies with unique capabilities. The customers' view was summarized as superior return-on-investment based on throughput and lower cost of ownership.

- **Product features—Whole product.** Mark column 1 if the dialogue considers only the capabilities of the new product. Mark columns 2, 3, or 4 as the discussion moves toward the whole or augmented product. Mark column 5 if the dialogue views the new product as one link in a whole-product chain of products and services that provide capabilities.

Example: Marked in column 2 because most of the discussion was on product features, but some time was spent on future upgrades, third-party add-ins, training, and repair.

- **Qualitative—Quantitative.** Mark column 1 if the specifications and market data lack numbers or precise nouns, adjectives, or verbs. Typical descriptions for column 1 are easy-to-use, low cost, high quality, and modern appearance. Mark columns 2, 3, or 4 as the specifications and market data include more numeric values and precise words. Mark column 5 if numbers and precise words are used. Note that some aspects of specifications and market data are important but impossible to capture in numbers or precise words. Examples are the market's perception of value or a product's "personality," like feel or image. The specifications and market data will be misleading if you exclude these aspects just because they lack precision.

Example: Marked in column 2. In this company, the easy-to-document specifications are numeric. Specifications for durability and software performance (the primary user interface) aren't numeric but introduce much dialogue.

- **Synthesis—Analysis.** Mark column 1 if the design is synthesized through a bottom-up approach and market data is synthesized

**TABLE 2: YARDSTICKS TO
EVALUATE COMMUNICATIONS PROCESS**

	1	2	3	4	5	
Checklist format						Matrix format
Less structure						More structure
Technology-oriented						Customer-oriented
Product features						Whole product
Qualitative						Quantitative
Synthesis						Analysis
Process-related						Product-related

from field reports and anecdotal information. Mark columns 2, 3, or 4 as the product depends on more top-down analysis and less on synthesis. Mark column 5 if the product is designed using top-down analysis and the market is analyzed with surveys and focus groups, or if the final product is based on analyses of technical feasibility and market interest.

Example: Marked in column 2 because the product was synthesized bottom-up from a series of existing building blocks for hardware, optics, and software. Top-down analysis was used to fit the blocks together considering throughput and the limits of physics. All market data was synthesized from field reports and anecdotal information.

- **Process-related—Product-related.** Mark column 1 if the discussion centers on manufacturing or business processes that support the product. Examples are assembly processes, software-development methods, field-maintenance methods, purchasing methods, and concurrent-engineering methods. Mark columns 2, 3, or 4 as the dialogue focuses more on the product than on supporting processes. Mark column 5 if the discussion is primarily on the product.

Example: Marked in column 4 because product accuracy depended on design and on the manufacturing processes used in-house and at suppliers. Most of the dialogue concentrated on product capability, some was on manufacturing processes (but none on software-development

methods), and a minor amount was on business processes, specifically field support.

The value of these yardsticks and the resulting footprints can easily be seen by comparing the example of ad hoc dialogue with an example of the QFD method

(Table 4). The footprints highlight how QFD differs from the ad hoc method.

MATRIX FORMAT USED

QFD employs a matrix format instead of a checklist format, so column 5 is checked for that yardstick. The middle section of the QFD matrix has two axes: the customer view and the technical view. The number of attributes per axis depends on the level of detail. Some QFD matrices have dozens of attributes on each axis. Other factors, like competitive products and technical specifications, are included at the periphery of the matrix.

In addition, the QFD matrix has specific locations for data, although the procedures for filling them in and interpreting the results aren't structured. Consequently, the structure yardstick is marked in column 4. The lack of explicit procedures makes it easy for users to get lost in the details—a frequent criticism of QFD. The matrix reserves specific areas for information like market potential, trade-offs of technical characteristics, and the relative importance of attributes.

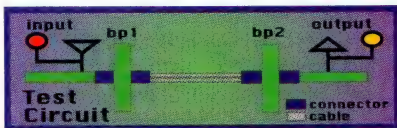
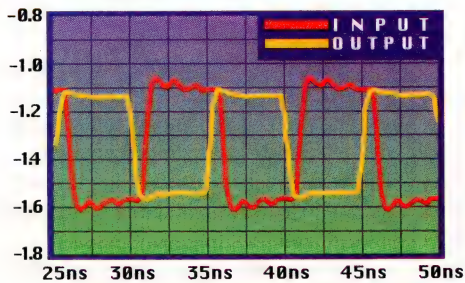
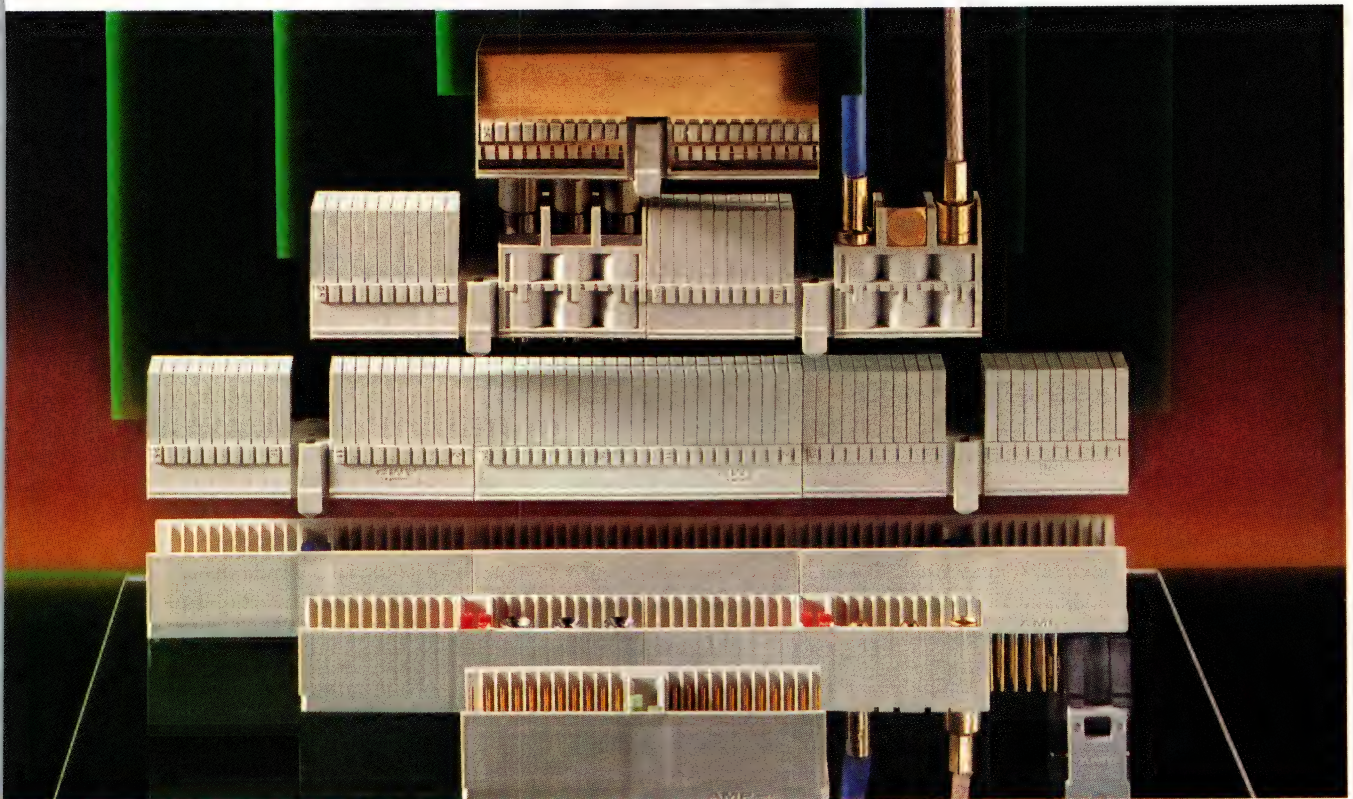
Moreover, QFD uses quantitative techniques instead of the qualitative ones typical of an ad hoc method. In fact, one important feature of QFD is its scoring system for comparing disparate product attributes like response time, field failure rate, and accuracy. Hence, that yardstick also rates a 5. The usefulness of the scores is enhanced by the precise use of words and numbers to describe these various attributes. The precision is the result of the multiple points-of-view that are a hallmark of a matrix format.

In fact, a limitation of QFD is its tendency to ex-

**TABLE 3: FOOTPRINT FOR AD HOC
METHOD OF DIALOGUE**

	1	2	3	4	5	
Checklist format	✓					Matrix format
Less structure	✓					More structure
Technology-oriented		✓				Customer-oriented
Product features		✓				Whole product
Qualitative		✓				Quantitative
Synthesis		✓				Analysis
Process-related				✓		Product-related

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clude specifications and market data that are difficult to capture in numbers or precise words, like a product's look and feel. If these aspects are important to the product, the results from QFD will be incomplete or misleading.

These three major differences between the ad hoc and QFD methods often are noticed by engineers who are just starting to use QFD. Their comments, however, are expressed as complaints: QFD is too complex (matrix instead of checklist), has too much red tape (far more structure), and favors details (more quantitative). In fact, these complaints are the strengths of QFD.

What's rarely discussed are the similarities between QFD and the ad hoc method. Both favor technology orientation over customer orientation. QFD attempts to strike a balance between customer and technology orientation by placing each on an axis. One or the other can dominate the discussion, depending on which has richer detail. Most companies have far more technical detail than market detail, so QFD favors a technology orientation (column 2).

Like the ad hoc method, QFD focuses on product features rather than the whole product (column 2). Most QFD matrices are for a single, shippable product, so the product's features appear on one axis and the customers' view on the other. No axis or space on the matrix is reserved for attributes of the whole product, which include the physical product, support services, and essential items from other suppliers. If attributes of the whole product are included in the product features or the customer view, they're usually dispersed and difficult to discuss as a complete package.

In principle, however, you can use QFD for any product, including a "whole product." That is, a chain of products and services which give value to customers. If you build a QFD matrix for the whole product, its features and the customers' view would appear on the two axes.

QFD and ad hoc also use

**TABLE 4: FOOTPRINT FOR
QUALITY FUNCTION DEPLOYMENT**

	1	2	3	4	5	
Checklist format					✓	Matrix format
Less structure				✓		More structure
Technology-oriented		✓				Customer-oriented
Product features		✓				Whole product
Qualitative					✓	Quantitative
Synthesis			✓			Analysis
Process-related			✓			Product-related

synthesis and analysis similarly. QFD captures bottom-up and top-down detail equally well, rating a 3 on the footprint. If the data along the two axes is well organized, a QFD matrix can support synthesis and analysis of both the customer and the technical views. Because at times you will want further analysis of the technical view, QFD has provisions for linking its technical view to other matrices for that purpose.

BALANCING ISSUES

Finally, the two methods balance process-related and product-related issues. The data included in QFD is product-related. However, you can link the technical axis to other matrices that focus on manufacturing or business processes. For this yardstick, QFD rates a 3.

The real limitations of QFD (and the ad hoc method) are the first two similarities. Both methods are short on customer-orientation and focus too much on product features rather than the whole product. Two other methods—the Product Value Matrix and Crossing the Chasm—don't have these limitations, but they possess other shortcomings (*Table 1, again*).

You must decide for yourself what an ideal footprint might be for your company, its engineers, and its marketers. A useful guide is a footprint based on concurrent-engineering principles (*Table 5*). A number of reasons make this footprint a preferred method of dialogue:

**TABLE 5: FOOTPRINT FOR PREFERRED
METHOD OF DIALOGUE**

	1	2	3	4	5	
Checklist format					✓	Matrix format
Less structure				✓		More structure
Technology-oriented				✓		Customer-oriented
Product features				✓		Whole product
Qualitative			✓			Quantitative
Synthesis			✓			Analysis
Process-related			✓			Product-related

• It features a matrix format that creates more thorough data and analysis. A major complaint of design and manufacturing engineers is that marketing data is anecdotal and its analysis is superficial.

• It has a formal structure that makes the process easier to replicate in other projects and less sensitive to the leader's or facilitator's skill level.

• It's customer-oriented. Most companies have a weaker sense of their customers than of the technology in their products. The marketing-engineering dialogue should strengthen the development team's understanding of its customers.

• It takes a whole product viewpoint, which includes the shipped product; sales, applications, and maintenance support; and essential items from other suppliers.

• It balances quantitative and qualitative methods of describing the product. The quantitative methods capture key attributes; the qualitative techniques capture the emotion of the purchase decision.

• It supports a top-down analysis of a proposed product and a bottom-up synthesis of it from related products and evidence in the marketplace.

• It encourages continuous improvement of products as well as manufacturing and business processes.

This ideal footprint is closer to the QFD footprint than the ad hoc footprint. Even so, major gaps exist between QFD and the ideal. QFD should be more customer-oriented, pay more attention to the whole product, and strike a better balance between qualitative and quantitative techniques. One solution is to use QFD in tandem with another method, perhaps the \$Appeals or Product Value Matrix (*Table 1, again*). Experiments on such combinations are in the works, but results have yet to be published.

Improving relationships with marketing can have a direct effect on design integrity, a universal goal for development groups. A product with design integrity makes sense as a whole.

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A thorough understanding of the market and technology is the first critical step toward design integrity, and footprints can help you achieve that goal. They help you move beyond superficial discussions with marketing to ones that consider customer and technical issues equally, that use quantitative and qualitative methods in appropriate ways, and that search out inconsistencies and hidden patterns in data to reveal ways of improving the design.

As engineering's relationship with marketing improves, footprints can keep you on track while you search for improved ways of discussing new products. □

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Don Stewart heads Concurrency Group, a consulting firm that specializes in new-product development issues. Stewart received his BSEE degree from Massachusetts Institute of Technology, Cambridge, and an MBA degree from Harvard Business School.

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OUR UNIX.

READER SERVICE 152

Putting Technology To Work

digital

CIRCLE 521 STREAMLINE YOUR WIEN BRIDGE

ERIC KUSHNICK

LTX Corp., University Ave., Westwood, MA 02090.

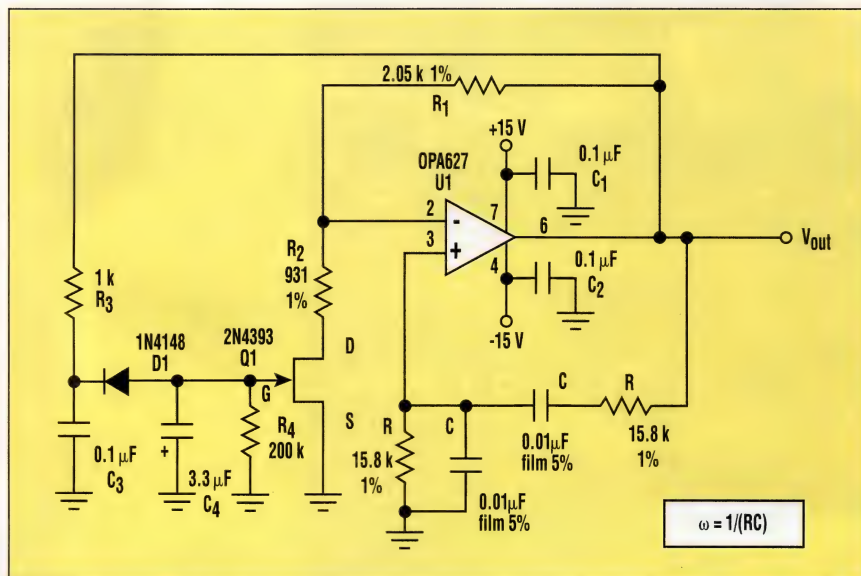
A Wien-bridge oscillator can produce a very low distortion sine wave at audio frequencies and beyond. It operates by carefully balancing a frequency-selective positive feedback with an equal amount of negative feedback around a high-gain amplifier. The amount of feedback must be continuously adjusted for proper operation. Some textbooks suggest a light bulb or a positive temperature-coefficient resistor for this purpose.

A FET can also do a nice job of controlling the feedback, but the ac voltage across the FET must be kept low to prevent nonlinearities from introducing distortion in the sine-wave output. The trick to overcoming these nonlinearities without sacrificing output amplitude is to use a resistor (R_2) in series with the FET (see the figure).

The two resistors (R) and two capacitors (C) comprise the frequency-selective positive feedback network, and set the frequency of oscillation: $f = 1/(2\pi RC)$. R_1 , R_2 , and the FET make up the negative feedback path. For the device to operate properly, R_1 must equal approximately $2 \times (R_2 + R_{FET})$, where R_{FET} is the effective resistance of the FET. R_2 must be small enough so that $R_2 + R_{FET}$ (minimum) is less than $1/2 \times R_1$, or the oscillator won't be able to start. The closer R_2 is to $1/2 \times R_1$, the less voltage will be dropped across the FET, and the lower the distortion at the oscillator's output.

The FET's gate threshold voltage controls the oscillator's output am-

plitude. R_4 and C_4 set the response of the gain control loop. The circuit given in the figure produces approximately 2.7 V p-p (about 1 V rms) of output at 1 kHz with a measured total harmonic distortion of better than -60 dB (0.1%). □



IN THIS WIEN-BRIDGE oscillator circuit, R_2 prevents FET nonlinearities from producing distortion in the output.

CIRCLE 522 DUAL V_{out} DAC TAKES LITTLE POWER

JOHN WETTROTH

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086;
(408) 737-7600.

By using a combination of power-conserving tricks, a dual voltage-output DAC draws less than 20 μA from a 5-V supply (see the figure). The circuit suits a need for programmable voltage generation in slow or static applications, such as the nulling of offsets in a micropower instrument.

Current-output DACs typically waste power by routing the complement of I_{out} to ground. In this setup, that waste is avoided by operating each DAC in the reverse voltage-switching mode. The reference voltage is applied to the pins normally labeled I_{out} .

The I_{out} pins possess a constant and relatively low input impedance of 11 k Ω . To reduce input currents,

the reference voltage is scaled by 100 (from 5 V to 50 mV), and therefore delivers only 5 μA to each DAC input. Signal levels are restored by a compensating gain of 100 in each output amplifier. Inexpensive 10 M/100 k resistor networks are a good choice for the multiple 100:1 attenuators required. Though only 2% accurate, they offer much better capabilities in matching and tracking.

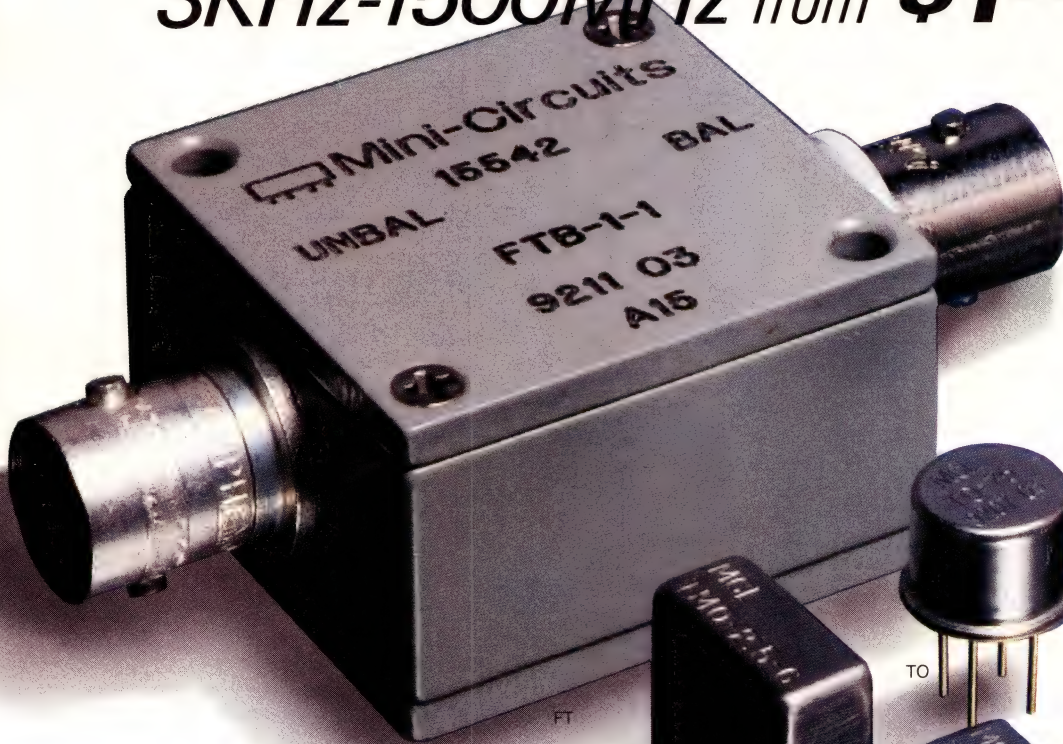
Greater scaling is impractical because of 0.5 mV (maximum) offsets in the output amplifier shown in the figure. Amplified by 100, these offsets produce worst-case output errors of $\pm 1\%$ (0.05 V). The errors are constant over temperature, but additional error due to drift over a range of 40°C is typically $\pm 1/2$ LSB. These

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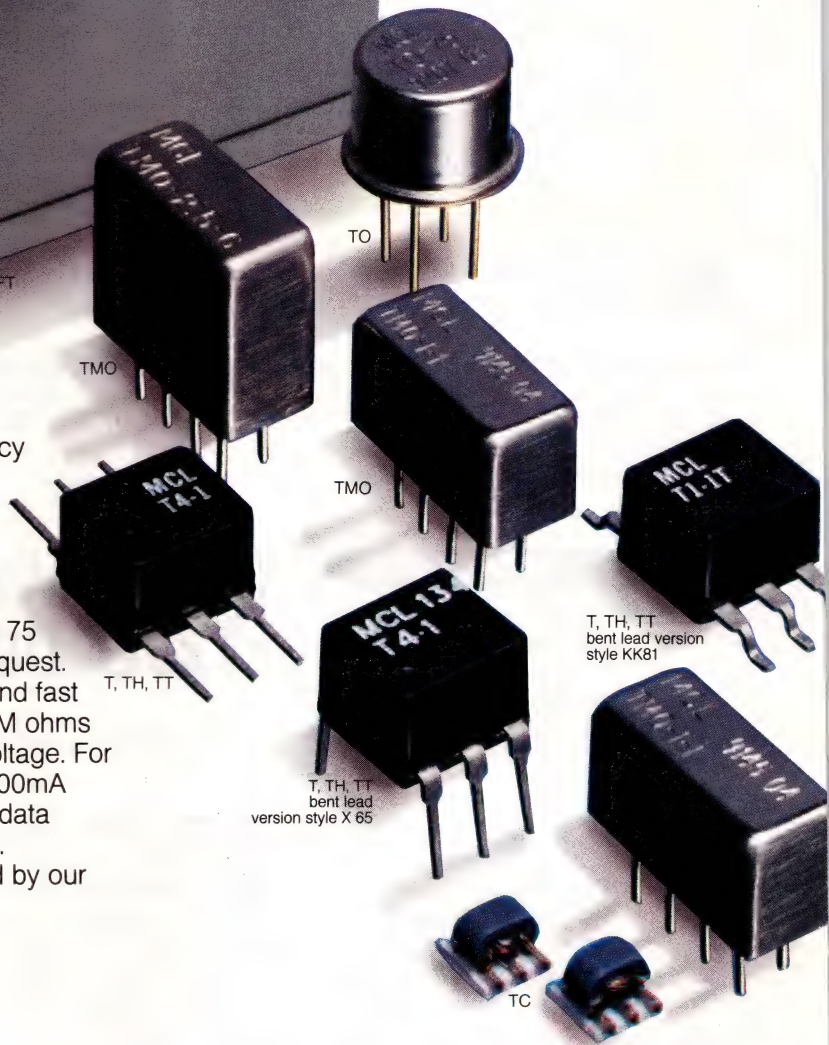
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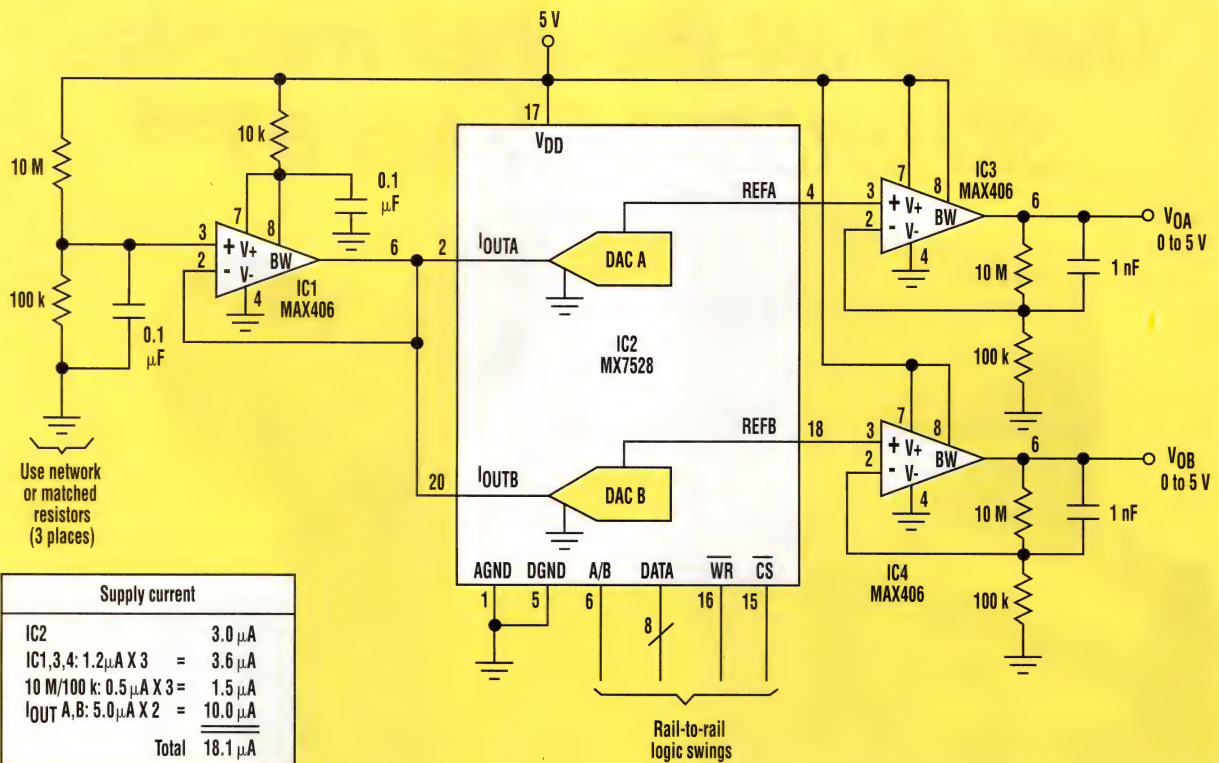
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F 71-Rev.E



THIS DUAL-DAC CIRCUIT, which provides two independent 8-bit DACs with voltage outputs and a common reference, draws less than 20 μ A from a 5-V supply.

micropower op amps are chosen for low supply current—their typical I_{DD} is only 1 μ A.

The last requirement for minimizing the overall current drain is to en-

sure that logic signals applied to the digital inputs of IC1 swing to within 0.2 V of each rail. The maximum specified I_{DD} for that condition is 100 μ A over temperature, but this speci-

fication (like most CMOS I_{DD} ratings) is extremely conservative. I_{DD} is negligible for rail-to-rail swings, but rises dramatically as the swings approach TTL levels. □

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a \$150 Best-of-Issue award.

IFD WINNER

**IFD Winner for
January 10, 1994**

W. Stephen Woodward, Venable Hall, CB3290, University of North Carolina, Chapel Hill, NC 27599-3290. His idea: "Get Absolute Temp Log with RS-232."

CIRCLE 523 WINDOW COMPARATOR DRIVES BICOLOR LED

DON BRAY

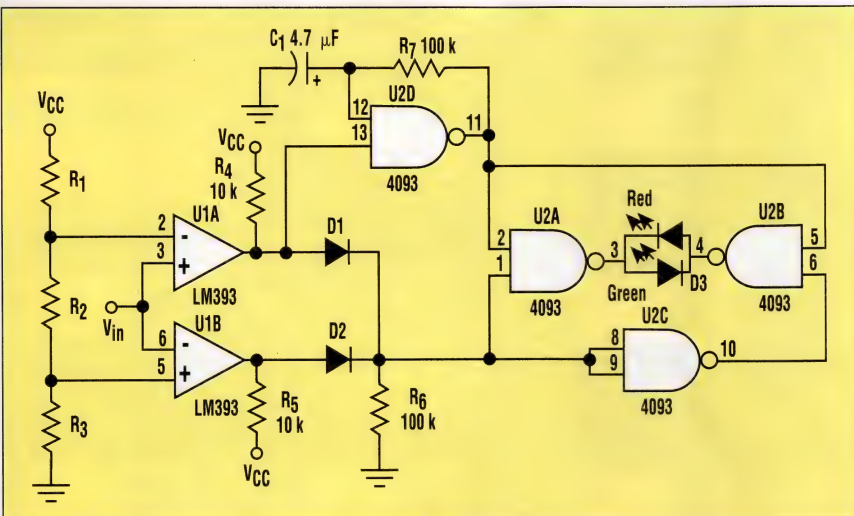
Horton Automatics, 4242 Baldwin Blvd., Corpus Christi, TX 78405; (512) 888-5591, fax: (512) 888-6510.

Using just one bicolor LED, this window comparator can display the status of an incoming voltage (see the figure). The LED is green when the voltage is within limits, red when it's low, and flashing red when it's high.

In the setup, U1 is wired as a conventional window comparator. Typically, both of U1's outputs are low when the voltage is in tolerance. As a result, there's a high at U2A-3 and a

low at U2A-4, lighting the green LED in D3. The flash clock, U2D, remains disabled because pin 13 is low.

If V_{in} falls below the acceptable limit, the output of U1B goes high. This flips the states of both U2A and U2B via D2, lighting the red LED in D3 to indicate an undervoltage condition. The flash clock still remains disabled. If V_{in} rises above the limit, U1A-1 goes high instead. This also flips the states of U2A and U2B via



A SINGLE BICOLOR LED is used to display the status of an incoming voltage in this window-comparator circuit. A green LED indicates the voltage is within limits. If it's red, the voltage is low; if it's flashing red, the voltage is high.

D1, lighting the red LED. However, U2D-13 also goes high and starts the flash clock, causing the red LED to blink. This signifies an overvoltage condition.

R_1 , R_2 , and R_3 are selected to give the desired window. Note that, for the flash clock to work, U2 must be a Schmitt-trigger device. D1 and D2 can be any small-signal diodes. □

EDITORIAL CALL WANTED: SOFTWARE IDEAS FOR DESIGN

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Put Our List On Your List

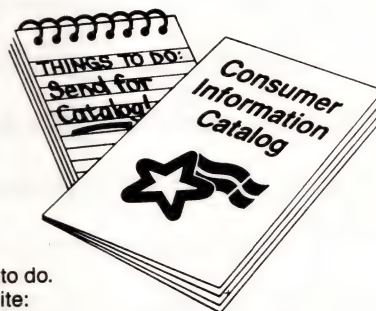
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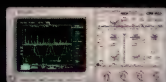
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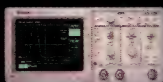
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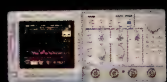
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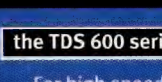
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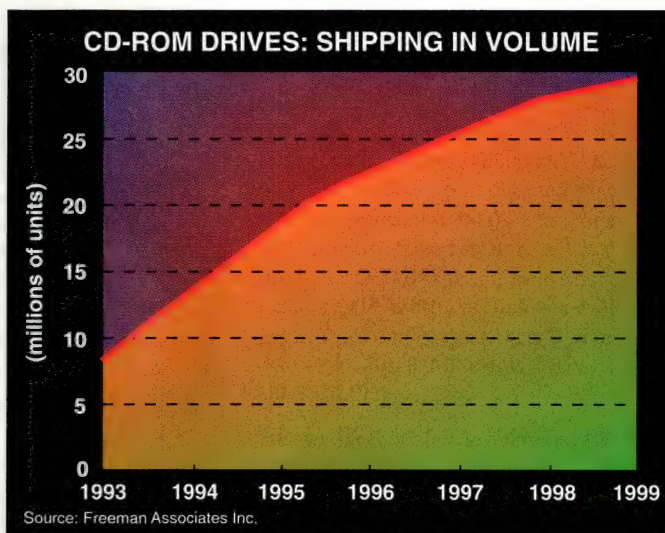
Tektronix

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Multimedia applications, a steady flow of new titles, along with declining costs for hardware, software, and disk replication are stimulating vigorous demand for CD-ROM disk drives, according to Robert Abraham and Raymond Freeman, authors of *Optical Data Storage Outlook*. The Santa Barbara, Calif., market researchers also say that 8.3 million CD-ROM drives shipped last year, with 13.6 million units expected to ship this year, amounting to a 63% growth rate. By 1999, shipments will amount to nearly 30 million drives, they predict. As with most electronic equipment, prices for drives are falling rapidly, with the fastest drives—those having access times of under 400 ms along with fast transfer rates—leading the market. Because of their dominance in the CD audio market, Asian manufacturers lead the production of CD-ROM drives; Matsushita had 24% of the industry's revenues last year; Sony had 23%, while Toshiba and Mitsumi had 14% each.



TALES FROM A SKUNK WORKS

In the past two columns, we've been discussing how to set up skunk works. Once everyone is up to speed and upper management is convinced that improving new product development is crucial, detail work can start. The place to start, however, is not with the skunk works. First, you must develop a road map: What products and markets do you want to compete in? How will you win? What are your firm's core capabilities?

Leaders have a clear vision of where they want to lead. Sun sticks close to the Sparc desktop, while Intel owns the PC desktop, and Microsoft covets mass-market software. When your strategic vision loses focus, as IBM's did, there is trouble ahead.

Strategic vision is a topic that consumes books and requires constant work. For this column, we will simply note that a deep, realistic understanding of goals and capabilities is necessary for success.

My view is that time-based new product competition in today's intensely competitive markets resembles the fast cycle "learning loops" of fighter engagements. Focus, target, niche, boom—the aggressors pound wave after wave of new products into the market. You don't dominate first-rate competitors with the first attack. Victory requires speed, persistence, and constantly pressing your advantage. (See, for example, the "Are We Missing Something?" chapter in *High Tech with Low Risk*.)

The winners seize the initiative and force their adversaries into reaction. Like a dog fight round and round they go with fast cycle products. Those who lag find themselves left with ever thinner margins to fund R&D and market knowledge. That is one reason we see so many low-margin, knock-off products. The best competitive advantages are superior technology and market knowledge. So if possible seize the initiative and make adversaries react to you or flee.

Most firms trapped into cost cutting and reaction can be forced into a downward spiral.

There are many books on fast cycle products, but one I like is my friend Marvin Patterson's, *Accelerating Innovation* (Van Nostrand, 1993). Hewlett-Packard seemed a bureaucratic and sluggish firm only a few years ago, until the company mounted a determined top-level effort to improve its new-product development processes. Now the company runs like a gazelle and pounces like a panther. HP arguably is now best in the world in the tough markets of computers and printers. HP's results were extraordinary, and Marv's book gives some of the models the company uses for the development process. Other books worth reading are Smith and Reinertsen's *Developing Products in Half the Time*, and Stalk and Hout's *Competing Against Time*.

Before you think of skunk works, you must be fully committed to winning the war, and you need to train. You need to tune up your corporate body, focus your energies, and make your new product development processes into best-of-breed. The key thing is to be able to move through fast product development cycles without sacrificing quality or incurring exceptional cost. You must be competitive at your core businesses before you reach for headroom and try to innovate. If you cannot crisply move cost-effective products into the market, you will waste the innovation abilities of a skunk works.

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. To order, phone (503) 280-8547.

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QUICK REVIEWS

An independent design handbook, the *Pentium Processor System Architecture* guides readers step by step through the microprocessor's architecture. Taking a systems viewpoint, the 306-page book was written by the team that conducts technical training about the Pentium for engineers at Intel, IBM, Compaq, Dell and other computer companies. The handbook begins with a chip overview and ends with how to test and debug it. It also has a 245-page quick-reference guide, an index, and 74 illustrations. The \$29.95 book is available by mail from the Order Desk, Computer Literacy Bookshops Inc., 2590 North First St., San Jose, CA 95131; (408) 435-0744; FAX-1823. **CIRCLE 462**

K M E T S K O R N E R

...Perspectives on Time-to-Market

BY RON KMETOVICZ

President, Time to Market Associates Inc.

P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804



How many times, to help predict the completion date of a new product development effort, have you been asked to provide best case, nominal, and worst-case, task-duration estimates? It's happened to me more often than I care to remember. The process of using this information usually goes like this... You supply your three numbers and others on the team supply their three responses to the project manager on a task-by-task basis using a highly scientific estimation process. You look at the task and say to yourself, "I can do that in 20 days." With nominal set, the mind goes to work thinking about what can go wrong to form a mental list. The list includes things such as "It doesn't work and I have to make it work," or "I made a mistake and I have to fix it." Soon a worst-case number starts to materialize—40 days starts to look good. Then you begin looking at the other extreme and think about how fast you could go if they keep you out of meetings, unplug the phone, and turn off e-mail.

Under these conditions, you convince yourself that you could do this task in 7 work days of uninterrupted time. And then it's on to the next task where you repeat the process. When you finish looking at all the tasks you are signed up to do, you turn in your numbers to the project manager. While you do your job of estimating, the other highly conscientious members of your team put forth the same quality effort. And as you finished your work, they finished theirs and gave the numbers to the project manager. You think the process they used was similar to yours but you do not know for sure—you worked in isolation.

The tasks for which you and your team member supplied duration data, of course, are networked and reside in a simple database. For each task, the project manager enters the supplied data. Using a sophisticated tool, the best, nominal, and worst-case numbers for each task interact to statistically compute the effort's range of end dates. When highly polished number-crunching tools are not available, the project manager goes through the database three times—once for best case, nominal, and worst-case task duration numbers. He/she then establishes the range of possible completion dates. I used the latter method to produce the following:

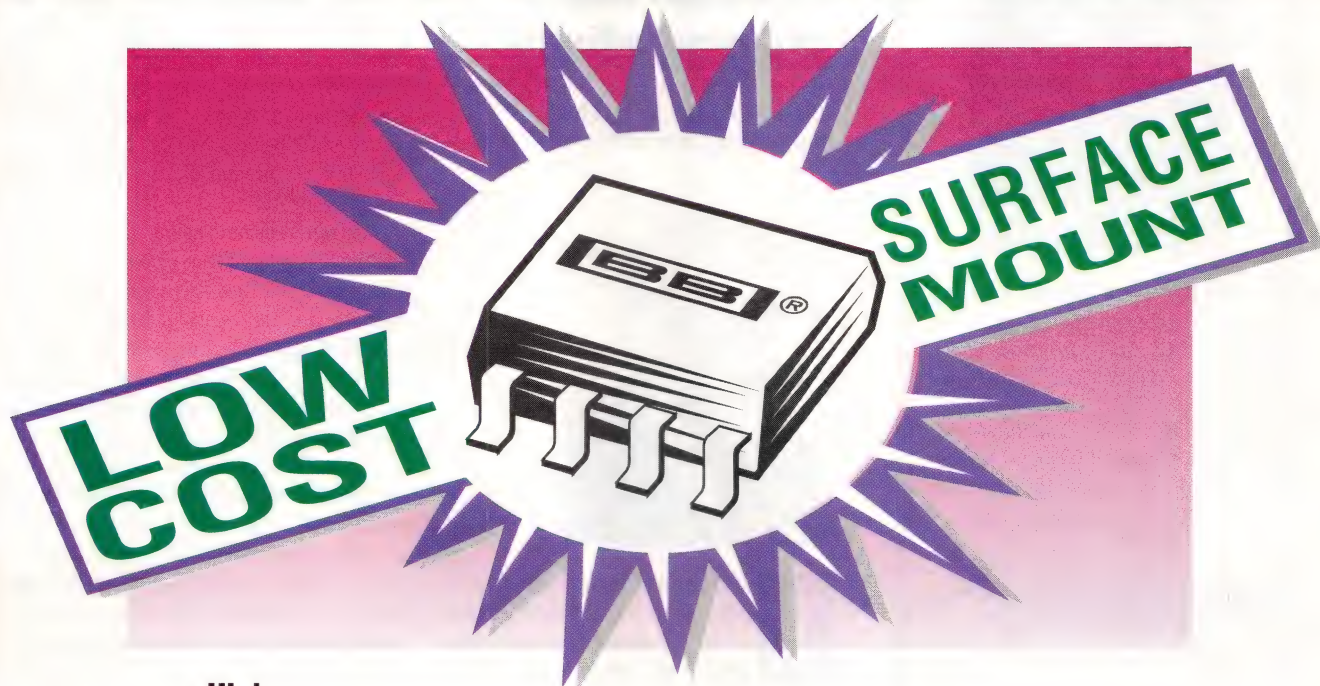
ID	Name	Duration (days)	1994												1995											
			J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D
1	Project best-case duration	200																								
2	Best case task statistics	200																								
3	Project nominal duration	300																								
4	Nominal task statistics	300																								
5	Project worst case duration	500																								
6	Work case task statistics	500																								

It shows a best-case duration of 200 working days, a nominal completion time of 300 days, and a worst case time of 500 days. Data like this gives the project manager a really big headache. Which case to use? If nominal is 300 days, what actions must be taken to get to the best case state? Or if worst case is 500 days, what has to go wrong to get to this sorry state. From the data the project manager has, he/she can't reliably answer these questions. Hence, when asked by executive managers to predict the future, nominal becomes the project managers fall-back position. Ahh, but then comes the pressure from management.

The nominal 300 working day duration is way out there. This group didn't get to where it is by thinking in nominal terms. Good executive managers will persuade the project manager to take the best-case prediction as the team goal, convinced it's the motivator the team needs. Then the project manager commits to the best case time! I've never seen this methodology work or produce a useful result. If you're using it, consider making a change—a database constructed in this manner is a one-shot exercise—we want to do better, much better.

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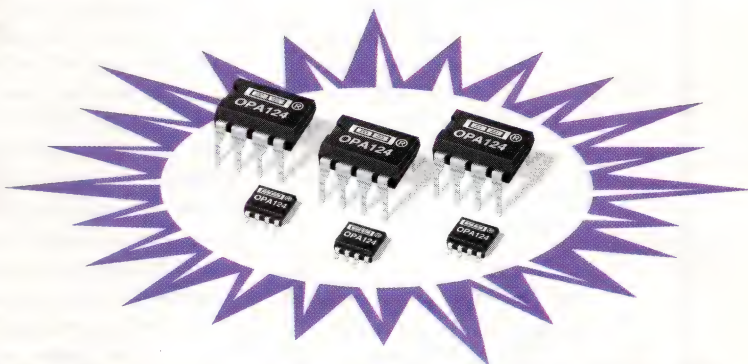
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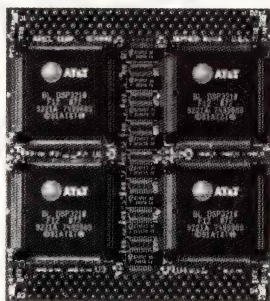
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...Straight talk and productivity

BY FRANK J. BURGE

Director of Market Development for Electronic Design



I must be getting grumpy as I get older. Or is it really more difficult to get a straight answer today than it was when I started out in this business.

Six weeks ago we move into a condo in a town called Los Gatos. After we move in, I notice that there is only one smoke alarm in the townhouse and it is in the upstairs hallway. So I call information for the phone number of the local fire station to get a recommendation on where alarms should be located. I dial the number supplied by the information operator and am connected to the fire district central office. The person on the other end of the line listens to my request and then suggests I call another number. I call the other number and explain what I am after. And again I'm told that they don't answer such questions but I should call the town of Los Gatos.

I call Los Gatos and am connected to a nice gentleman. I ask him for a recommendation and he explains that it depends when the place was built and whether or not any major renovations have been made in the past ten years. Huh? He then tells me that the town had attempted to pass a smoke detector ordinance but the local Board of Realtors fought it on the grounds that the Los Gatos ordinance was more restrictive than the California law. Nutso. Now I have a legislative history of the smoke alarm issue but no recommendation. Finally in desperation I call my barber, who tells me what to do. My barber is one smart cookie.

While I'm mulling over how tough it is to

get a straight answer these days, I see an ad for a hot new semiconductor product that claims to be the "world's fastest." I see this "world's fastest" description quite often these days. Anyway I am curious about the applications in which the world's fastest gizmo might be used. So I call a friend at the company manufacturing the product and ask the question.

My friend seems evasive, which gives me the impression he doesn't have the foggiest idea who might use this product. But certainly if it is the "world's fastest," the assumption is all sorts of people will want to use it. Huh! Since I keep pressing the issue, my friend suggests I call the 800 number in the ad. When I call, I am put on hold for several minutes. Then someone comes on the line and starts questioning me. Where had I seen the ad? Finally I get to ask my question about possible applications and am told I'll have to call another 800 number for that kind of information. This is beginning to feel like my smoke detector experience all over again. So I dial the new 800 number. And again I am quizzed but finally get to ask my question. The person at the other end of the line excuses himself to look up the answer. He comes back on the line and explains the "world's fastest" gizmo is for high-speed applications. I say thank you and hang up.

My smoke detector and world's fastest gizmo experience starts me thinking and I recall the recent news that U. S. productivity increased 6% in 1993, a remarkable gain. But with all the layoffs associated with the downsizing blitz, it's expected that productivity (revenue per employee) would be up since that's one of the reasons for all the layoffs. And if revenues increase at the same time people are being axed, then productivity increases even more. But just think of the possible gains in productivity if we didn't have to waste so much time getting a simple answer over the phone. Maybe we'd get our question answered on the first try—one might even call it the "world's fastest" telephone response system.

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BOB'S MAILBOX

Dear Bob:

I have stood on the sideline watching the degree vs. no-degree issue rage on in your column, and have often been tempted to write, but finally I am galvanized to write after reading the letter by Cory Hamasaki in the Dec. 2, 1993 issue. First I would like to say that I have worked as an electronic technician for over 10 years, during which I have worked in all aspects of computers and electronics. I have also spent the last 12 years attending classes part time, working toward a BSEE degree, while working a full-time position.

I take exception to several points Cory Hamasaki stated as fact, but which my extensive experience has shown to be false.

The statement about testing out of lower-level courses for credit is misleading. To test out of a class, a student must take the equivalent of the final exam for that particular class. Due to the theoretical approach of engineering schools, this test will invariably test specific mathematical analysis approaches to electrical circuits. Only diligent and lengthy individual study, or taking the class, will provide this specific information. Testing out of classes is not an option.

The statement about credit for work experience is totally misleading and false if the school is accredited by ABET. ABET specifically does not allow credit for work experience, but only for transfer credit from approved programs. Independent study is allowed for three or four credit hours at most engineering schools, but so far my inquiries have received the response that previous work would not apply.

Also, almost no credit I earned towards my Associate degree in electrical engineering technology was transferred towards my Electrical Engineering degree. ABET has ruled that technology and engineering shall never be intermixed.

The statement that a school would tailor a program if you work with them is ridiculous. I know of no school that would waive their specific graduation requirements. Certainly at the schools I have attended, the Engineering programs clearly define and specify which classes one must take to graduate. There are technical electives that one has the leeway to select to pursue a field of specialization, but these are often the most demanding and difficult classes in the program.

The statement about the professor having real expertise made me laugh. In the last few years, I have learned how not to correct my professors. I realized that this was not helping me get my degree.

In my applied design classes, I now let the professors state whatever false, out of date, and misleading information they want to, and I readily regurgitate this false information on homework assignments, and on tests, so that I get the correct grade. My experience has been that the only time I have not had greater knowledge of the material than the professors has been in the case of my theoretical classes.

The statement about your employer paying for tuition and allowing time off from work also is misleading. It is true that my current employer allows me time off from work so that I may attend classes. They also require me to make up all the time I take off to attend class. Previously, when I worked for a major computer company in a research laboratory, they allowed me time off to attend classes, and paid for my test books and tuition. Sounds great, but the reality has been, and continues to be, that I was resented by my management for taking advantage of this perk.

Certainly, the company's needs have always been expected to come first, regardless of exam or school project assignments. I remember while I

was working there during the semester I took chemistry and differential equations, I was expected to finish a project at work on schedule. This entailed my being out of state frequently during the semester, and often being expected to work 60-hour weeks. Yes, I completed my project on schedule, but my grades certainly reflected the time I was allowed to pursue my school work.

With all this griping, you may wonder why I continue to pursue this degree. It is because I am tired of having to prove the hard way that I know what I am doing. I am tired of having people automatically close the door in my face because I do not have a degree. Currently, I am the Laboratory Manager for a small computer research company, but I am only begrudgingly allowed to perform design tasks, as I am not an engineer.

Recently, I have had design consulting opportunities that I learned more from while performing my job than I have learned from all my classes. But I will persevere, so that hopefully sometime soon I too can put BSEE after my name.

Thanks, Bob, for writing such an insightful column. It's always refreshing to read something so firmly grounded in reality

WILLIAM C. SCHNEIDER
Blacksburg, Va.

I figured that it would turn out like this. Good luck on your degree work—and on your REAL education.—RAP

Hi Robert:

I was reading your column on "Technical Reading Stuff" in the March 7 issue, and much to my surprise I noticed that you had a question about books on printed circuit design. There are currently two books covering this subject that I can recommend highly to those who would like to do some real art and get away from the mechanical humdrum of CAD design software.



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A public service of this magazine

PEASE PORRIDGE

Both of these books were published by Bishop Graphics, which is now owned by Chartpack Co. I do believe they are still available, however. The books are titled *Analog Printed Circuit Design and Drafting* and *Digital Printed Circuit Design and Drafting*. Both are by Darryl Lindsey and should be available from Chartpack for about \$60.00 apiece. A beginner's layout kit used to be available from Bishop for both texts, but I don't know if that's still the case.

Any person that reads these books will find they are well written, although details on why things are done thus and such are sometimes scant. These books are oriented toward the artistic as well as the practical user with 3-color plates illustrating the art masters, and exercises to boot. As a professional "layout/designer" type I would recommend these books for anyone who is at an entry or advanced level.

The one piece of advice I can give to anyone who wishes to pursue board design is know how to draft by hand (as well as by computer) first. To achieve elegant as well as functional layouts that are logical, one must be a lot of artist, with very little engineer/designer.

It takes a God-given talent to really excel in laying out boards that are superior to PC-generated objects, but anyone can benefit from the knowledge contained in these volumes.

ALAN C. BOYLE

Bakersfield, Calif.

For some aspects of layout (grounds, noise, crosstalk, interference), the engineer's insights are still quite important. We found where to order those two books, and also a book on Surface Mount Technology (\$72.40). Call Fine Line Photo at (800) 560-8400. I'm buying all three books.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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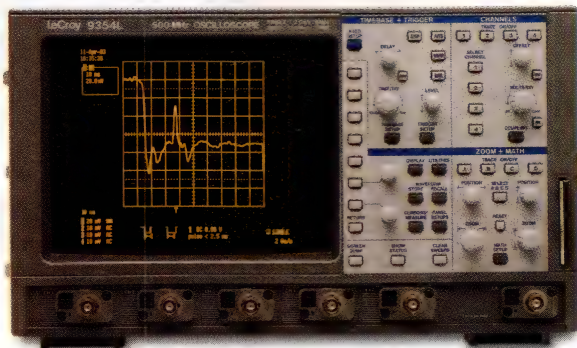
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READER SERVICE 178

COMPUTER SYSTEMS

A SPECIAL EDITORIAL FEATURE

PLUGGING INTO PCMCIA

MULTIFUNCTION CARDS

BILL GURNEY, NATIONAL SEMICONDUCTOR CORP.

The PC industry seems to be gradually embracing the PCMCIA standard as the expansion option for the future. With its compact form factor and ruggedness, PCMCIA lets users add functionality without removing the systems' covers. One area of specific interest is to offer multiple functions on a single card. Because the emphasis for PCMCIA rests mainly on portable systems, multifunction cards let designers reduce the number of slots that are required in the system.

Multiple functionality has its challenges, though. A proposal that's currently on the drawing board of the PCMCIA committee's Multifunction working group should address these issues, especially those present in 80X86-based systems. One particularly sticky issue involves the sharing of an interrupt signal (IREQ) on the PCMCIA I/O interface.

Sharing the IREQ line can cause problems when more than one client device driver attempts to use the line. The system first must identify which function actually requires service, then determine how to call the correct interrupt service routine (ISR) to handle the interrupt. Because many ISA-based PCs don't define a protocol for interrupt sharing, the client device drivers simply "steal" the interrupt vector. This action of not keeping the vector that's being replaced could cause the total loss of a valid pointer for an already existing client. A possible solution is to supply a monolithic client device driver to determine the interrupting source and service the interrupt. But this approach is undesirable if only one function is operational. Designers must decide whether or not memory should be sacrificed for a multifunction driver.

If approved as written, the proposal from the working group will specify changes to both the card's hardware and the host system's software so that independent client device drivers can share the multifunction card. To address the issue of concurrent function operation, and ultimately concurrent interrupt generation, the card must implement a mechanism that allows two or more functions to interrupt concurrently and have both interrupts recognized by the system. On the system side, modifications to Card Services will address the processing of the received interrupt.

The interrupt sharing requires a unique hardware solution to effectively queue up interrupts from the card's active functions. Due to the positive-edge requirement of the programmable interrupt controller (PIC), the card-interface IC will need to perform the appropriate sequence of interrupt generation. To achieve this, two bits each will reside within the Configuration Status Register (CSR), IntrReset, and Intr. When IntrReset is reset to 0, the Intr flag represents a function-specific interrupt and is cleared by the function, not by the host. When it's set to 1, the function requires positive acknowledgement that the interrupt event was completely processed by the host. The acknowledgement is given by the host resetting the Intr flag.

If any function on the card then requires service, another interrupt must be generated. Because the card must signal an interrupt condition whenever any function requires service, the Intr bit should be aliased for all functions that reset the IntrReset bit to 0.

In addition to the hardware changes, alterations to the software are required, particularly to the Card Services. The biggest changes include an interrupt redirector and modifications to the parameters passed to the Card Services function calls. The redirector is required because the end-of-interrupt (EOI) processing on the PIC must only be performed once. The outlined method states that Card Services receives the interrupt notification and routes the dispatch to the handlers.

When the routine is complete, Card Services performs the EOI processing, resets Intr in the CSR, and returns from interrupt processing.

Interrupt handlers for multiple-function PC cards are required to register with Card Services using an extended version of function RequestIRQ. The argument packet needs one extra 4-byte field that targets the handler's entry point. Complications can arise when using a generic enabler that's enabling the card for a non-PCMCIA-aware client. In this case, the generic enabler must register a redirection routine that transfers control to the appropriate handler by simulating the hardware event. Because many legacy handlers will perform EOI processing, a new flag in the Attribute field indicates that the interrupt routine (and not the Card Services) will perform the EOI processing. However, only one of these handlers will be allowed, with the other being PCMCIA-aware.



Reprogrammability Eases PCMCIA Designs

FPGAs allow design changes to be incorporated more easily.

BY CLARK WESTMONT AND BRIAN WALL

Xilinx Inc., 2100 Logic Dr., San Jose, CA 95124, (408) 559-7778.

PCMCIA-card designs emphasize standards compliance, yet implementation variations and expected standard revisions are causing turmoil within the industry. On top of that, market uncertainty and competition place a premium upon flexibility, product differentiation, and rapid time-to-market. In this unsettled environment, in-system reprogrammability can be a valuable tool.

Because the PCMCIA marketplace is growing rapidly, essential product features may spring up during the design cycle, thus necessitating design changes. But tight design schedules mean that changes must be executed quickly without impacting board layout. If an extender card or other debug vehicle with reprogrammable logic is used, changes can be made and monitored while the card is in-system, allowing immediate verification of the design change.

PCMCIA I/O cards often use a combination of chip sets, glue logic, and memory to accomplish their function. In many cases, the glue-logic portion of the design is implemented using programmable logic, such as field programmable gate arrays (FPGAs).¹ PCMCIA functions that can be incorporated into an FPGA include I/O addressing control, Card Information Structure (CIS) control, configuration registers and controls, reset, power down, interrupt control, and Wait generation. Depending on the FPGA's size, other application-specific logic also can be included into the chip.

The CIS describes the card's capabilities and specifications.

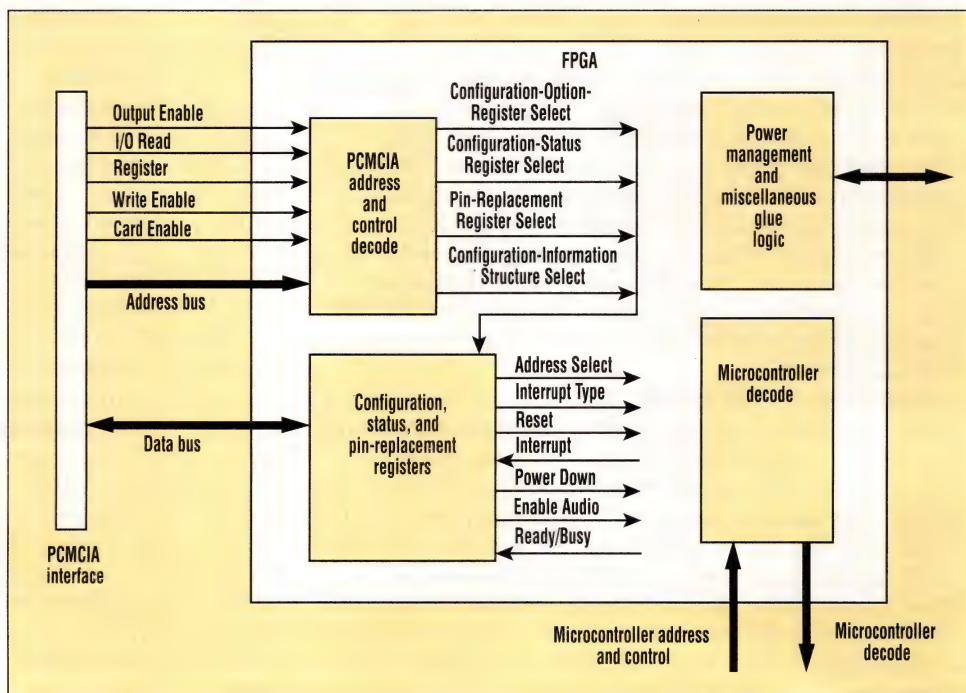
and offers a standard method for the host system to determine card-specific information. All cards that are compatible with the PCMCIA 2.0 standard must have at least one card-configuration register to control the card's configurable characteristics. All of these are read-write registers, one byte in size.

Virtually all of the PCMCIA interface control logic implemented in a data-fax modem, for example, is contained in the FPGA, plus the glue logic to tie together the fax-modem IC, the microcontroller, the RAM and ROM, and the UART (*Fig. 1*).² The functions could be handled by other forms of digital logic, such as gate arrays. However, the in-system reprogrammability is particularly useful in the PCMCIA setting for several reasons: field upgrades of the card; mutually-time-exclusive

functions; accommodation of platform differences with the same hardware design; and in-system design iterations during the development cycle.

There's a good chance that a PCMCIA card shipping today will be driven to obsolescence either by competing products or by revisions of the PCMCIA standard. Card power management is one area that's in flux and could change the minimum acceptable capabilities of the card. Reprogrammability offers a hedge against that risk by enabling field upgrades. Such upgrades require innovative use of FPGA reconfigurability. An FPGA can be configured in various ways. For most PCMCIA designs, the FPGA configuration file is stored in the same EPROM as the CIS. The PCMCIA standard requires the

1. When employed in a PCMCIA-based fax-modem, the FPGA contains virtually all of the PCMCIA interface control logic. It also holds the glue logic required to tie together the fax modem IC, the microcontroller, the ROM and RAM, and the UART.



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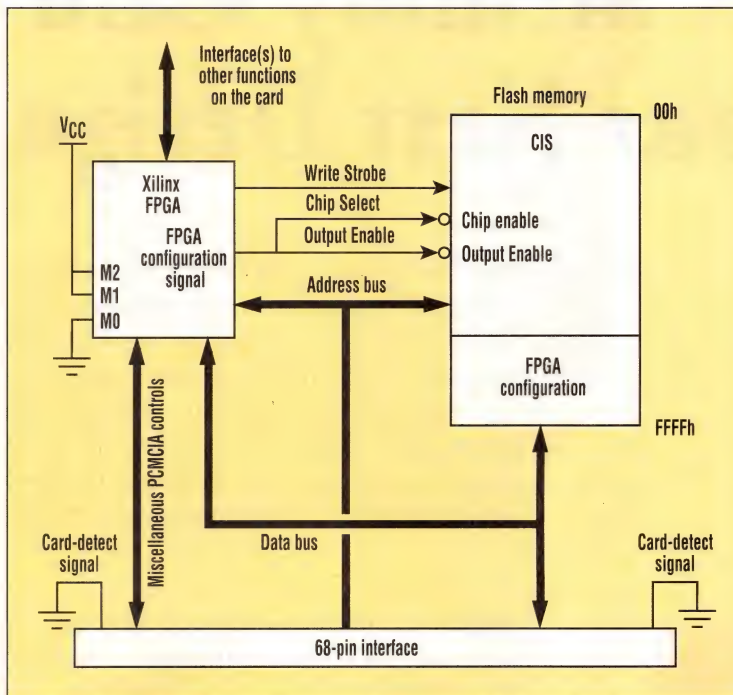
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REPROGRAMMABILITY FOR PCMCIA



2. This chip, which employs a Xilinx FPGA, resides in master parallel mode. A byte-wide flash memory stores both the CIS and FPGA configuration. The top of the memory block (FFFFh) holds the FPGA configuration. The FPGA's LDC pin acts as the chip and output enable for the flash memory.

CIS to reside at address 00h, so the FPGA configuration must reside above this memory block.

Because the FPGA configuration memory can be stored at virtually any address except that occupied by the CIS, it's able to be stored in flash memory on the card. This block of flash memory would be accessed by the host system only when the FPGA configuration is subject to change. Modifications to the FPGA configuration memory don't impact the FPGA's operation until a reconfiguration cycle is triggered. Thus, a card can receive new configuration information, but continue operation in the old configuration until the user is ready to initiate the upgraded program.

By employing the FPGA in master parallel mode, where M2:M1:M0 = 1:1:0, a byte-wide flash memory can store both the CIS and FPGA configuration (Fig. 2). The top of the memory block (FFFFh) is used for the FPGA configuration and accessed downward from that point.

The FPGA's LDC (FPGA configuration signal) pin acts as the chip and output enable of the flash device. To update the con-

figuration in the flash, the data bus passes the appropriate command to the FPGA; the write strobe, chip select, and output enable are turned on to the flash; and then new data is passed across the data bus to the addresses supplied by the address bus. The CIS also can be updated in a similar fashion. Programming details for the flash memory are found in the manufacturer's specification.

Upon card reset, the FPGA loads in the new configuration data and immediately begins performing the new program. The FPGA automatically supplies all addressing mechanisms required for configuration loading. Upgraded features, new host-interface support, bug fixes, patches, or other changes can be added this way as well.

The capability to support field upgrades also can be included in the card software that's resident on the host system. Upgrades could be distributed using floppy disks, which allows users to handle the upgrades themselves.

Upgrades offer evolutionary improvements that let customers protect their investment and

allow the company to keep its installed base intact. Upgrade capability is a prime selling point, mitigating customers' fear of product obsolescence. This capability also improves the shelf life of product inventory, as product revisions can be retrofitted to existing stock.

Unlike adding evolutionary improvements to the card, another approach, called mutually-time-exclusive (MTE) operation, enables the card to undergo wholesale personality transplants. MTE functions can be swapped into and out of the FPGA as needed.³ For example, a fax card needs to send or receive faxes, but never both simultaneously. As a result, an FPGA within a fax card could be configured to perform one set of functions when sending a fax and another set when receiving.

Another example of MTE is to initialize the card with the IEEE-1149.1 Boundary Scan Test Logic Standard to confirm card integrity, and then reload the FPGA with the logic required for normal system operation.⁴ Although some FPGAs are built with boundary-scan registers that meet the standard (like the Xilinx XC4000 family, for example), it's possible to emulate the external test mode, EXTEST, in a reconfigurable device. Four pins must be dedicated to the Test Access Port (TAP): TDI, TDO, TMS, and TCK. The FPGA can then create the instruction, bypass, and test-data registers; the TDO buffer; the TAP state machine; and other miscellaneous logic. This logic-efficient approach uses logic resources for test, then again for normal card operation.

Another use of reconfigurability allows the card to adapt to the host system's nuances. This is particularly valuable given the various implementations of the PCMCIA standard. Because there's neither established compatibility testing nor certification for PCMCIA cards, it appears that

■ REPROGRAMMABILITY FOR PCMCIA ■

the standard is as much platform-specific as it is platform-independent.⁵

It's beneficial to point out some of the possible reasons for differences in the PCMCIA interface implementation. For instance, the Motorola/Intel dichotomy of big-endian versus small-endian (in small-endian, the byte address of a word or double word is the address of the least-significant byte) is an obvious cause of problems. Data and address exchanges are critically dependent upon which assumption is employed. However, differences even exist among platforms based on 80X86 microprocessors. For 8-bit transfers across a 16-bit bus, the data might be on the high or low byte. Host PCMCIA controllers also can vary in the interrupts that are supplied to the card. Moreover, the WAIT generation may differ.

Variations also occur in how Card or Socket Services are implemented. In some cases, the supporting card software need only supply client information. In other cases, card software needs to define resource management, right down to the BIOS level.

The most straightforward approach to dealing with host differences is to bundle the known configurations (on a floppy disk) with the card. When the user is ready to apply the card in a system, the host system can be selected from a list of supported platforms. The enabler software is then able to handle host-side adaptation, while a custom FPGA configuration can be downloaded to the card to optimize the fit between the card and the host. As new host configurations become known, they can be added to the floppy disk or made available using a bulletin board system. A more sophisticated approach would be for the card-enabler software to query and detect system-specific information.

Platform independence also can be incorporated into the

FPGA during the development cycle. When Socket Communications Inc. was developing its PCMCIA Ethernet LAN adapter, the company distributed prototypes of the card to leading PC BIOS makers who play a critical role in implementing PCMCIA system software.⁶ Reprogrammability allowed the company to make same-day, in-system design corrections in response to the BIOS vendors' feedback.

Thanks to Mark Bowlby for his help with this article.

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Clark Westmont, an FPGA product manager at Xilinx, holds a BSEE from the University of California at San Diego, and an MBA degree from the University of California at Berkeley.

Brian Wall, a field applications engineer for Xilinx, received a BSEE from Boston University.

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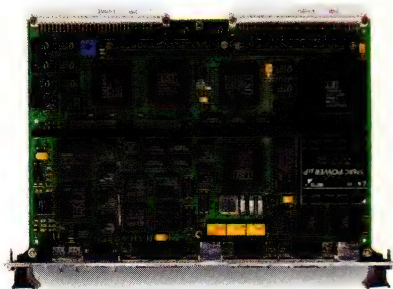
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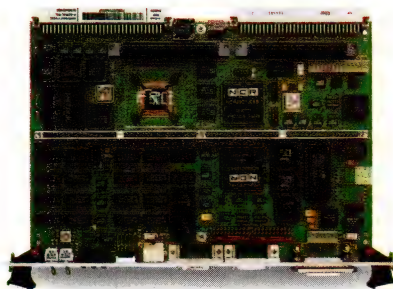
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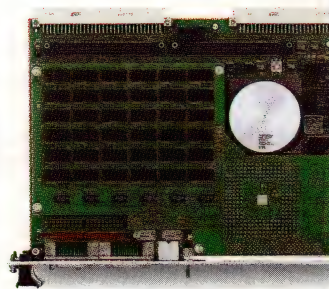
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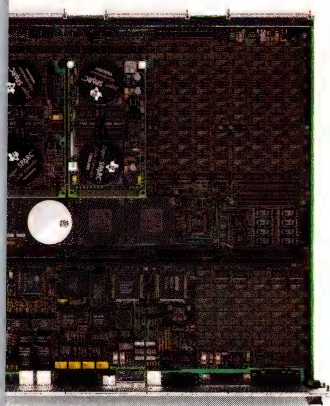
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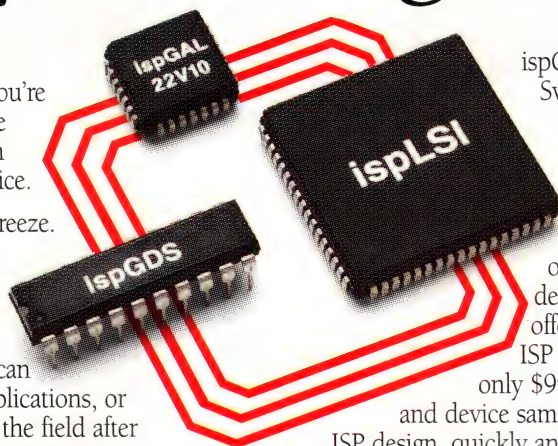
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SYSTEM DESIGN NEWS

A licensed DSP core, developed by the DSP Group, Santa Clara, Calif., will soon find homes in PC audio cards and other multimedia accessories. Integrated Circuit Systems Inc., Valley Forge, Pa., has licensed the Pine DSP core technology and the accompanying TrueSpeech voice-compression technology from the DSP Group. It plans to quickly bring to market low-cost multimedia audio building blocks that can use human speech to drive applications, such as voice annotation of E-mail messages. The TrueSpeech technology has been selected by Microsoft as the voice-compression technology for Windows-based personal computers. Other companies—Compaq Computer, Silicon Systems, and most recently, Motorola—also have licensed the scheme for other audio applications. Motorola, for example, plans to include the compression scheme as part of its PC Media product line, which it unveiled last month at Microsoft's Windows Hardware Developer's Conference. With TrueSpeech, captured speech files can be compressed with no noticeable degradation, minimizing the amount of memory needed for stored audio and the amount of data that must be transferred over E-mail networks. For instance, one minute of speech can be compressed to just 60 kbytes. Competitive compression schemes can't squeeze down the file sizes as much without significantly degrading the sound quality. Contact ICS at (215) 630-5300 and the DSP Group at (408) 986-4300.

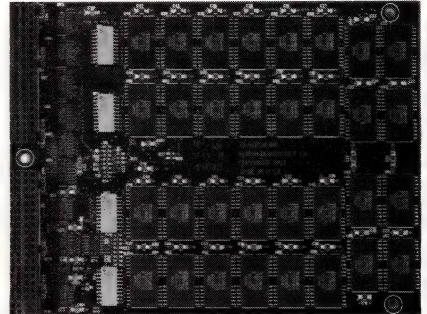
Software support is mounting for the Macintosh PowerPC platforms recently unveiled by Apple Computer, Cupertino, Calif. At the system introduction, over a dozen companies disclosed their software plans to offer native versions of their applications on the PowerPC RISC processor. Aladdin Systems, Watsonville, Calif., unveiled archiving, compression, and installer products, while many development-tool suppliers reinforced their commitments. Some of the other companies include Absoft, which offers MacFortran II, a C/C++ compiler, a multilanguage debugger, and the Cray/Absoft Fortran 90 compiler; Bowers Development, which has the interface builder and code generator; Echo Logic and its binary software translation package; Language Systems, which offers Fortran and Pascal compilers; and Metroworks, a supplier of integrated development environments and PowerPlant, an object-oriented application framework. Other software will come from Adobe Systems, ACIUS, Aldus, Claris, Denebe Software, Frame Technology, Insignia Solutions, Microsoft, Quark, Specular International, and WordPerfect. In addition, Ashlar, Sunnyvale, Calif., will offer free PowerPC upgrades of its Vellum 2D and 3D design and drafting software packages. Contact Apple Computer at (408) 996-1010.

The PCI bus is quickly gaining momentum as the local bus of choice, prompting motherboard designers to search out higher-performance chip sets to match with their 486-based microprocessors. With Intel's release of the 82420ZX and 82420EX PCIsets, they may not need to look any further. The second-generation chip sets supply a complete top-to-bottom solution, and can even handle the recently announced 486DX4 processor. The 82420EX, targeted at entry-level systems, consists of a PCI system controller (PSC) and an ISA bridge (IB). The chip set integrates a DRAM controller and a Level 2 write-back and write-through cache-memory controller. The 82420ZX PCIset consists of three chips: a cache DRAM controller (CDC), a data-path unit (DPU), and a system I/O (SIO) chip. The CDC, which includes an interleaved DRAM mode, bridges the CPU to the PCI bus. The DPU features four-level CPU-to-DRAM and CPU-to-PCI write buffers as well as a two-level PCI-to-DRAM write buffer. The SIO forms the bridge between the PCI and standard I/O buses. Samples of the both PCIsets are available now. In 10,000-unit quantities, the 82420EX sells for \$25.20 and the 82420ZX costs \$38.50. For more information, call Intel at (800) 548-4725.

SYSTEM DESIGN PRODUCTS

▼ MEMORY BOARD HOLDS UP TO 256 MBYTES

Application programs won't run out of memory with the FT200-Memory, a 256-Mbyte expansion board. To reach the 256-Mbyte level, two 128-Mbyte daughterboards are attached to a baseboard. The memory boards contain 60-ns DRAM, using 16-Mbit ICs. The baseboard houses an i860



processor to manage the memory. When installed in a VME system, the memory is accessible from the VME host as if it were a VME-slave memory system. In an ISA-based computer, the subsystem is accessible through PC I/O space transfers. Pricing for a 32-Mbyte configuration starts at \$5200.

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► CIRCLE 601

▼ HIGH-RES BOARDS OFFER 1.6-MILLION 2D VECTORS/S

Compatible with previous members of the GX family, the TGX200 and TGX400 graphics-accelerator boards are designed with resolutions up to 1920 by 1080 pixels. Graphics performance of up to 1.6-million 2D and 440,000 3D vectors/s are attainable, making the boards suitable for imaging and animation applications. The difference between the two boards lies in the amount of on-board memory—the TGX200 comes with 2 Mbytes, while the TGX400 offers 4 Mbytes. Features include an 8-bit color frame buffer that displays 256 simultaneous colors from a palette of 16.7 million. Available now, the TGX200 costs \$3100 and the TGX400 costs \$3400.

Aries Research Inc.

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Fremont, CA 94538
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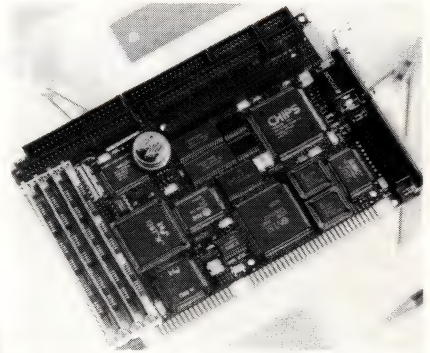
► CIRCLE 602

SYSTEM DESIGN PRODUCTS

▼ PC/AT BOARDS FIT HALF-SIZE FORM FACTOR

Two half-size PC/AT single-board computers, the VIPer800 and VIPer801, can be configured with 16 Mbytes of DRAM, 1 Mbyte of bootable flash EPROM, and 1 Mbyte of static RAM. The 4.8-by-7.1-in. boards are built with local-bus Super VGA support on-board to drive CRTs (VI-

Per800) or flat-panel displays (VIPer801). Configuration options include an Intel 386SX or a Cyrix 486SLC microprocessor. Other standard functions include keyboard and floppy-disk controllers, IDE and SCSI support, and a PC/104 expansion header for customization. A bundled software utility, VIP-UP, lets users customize the boards'



firmware. The VIPer800 starts at \$945, while the VIPer801 sells for \$1045.

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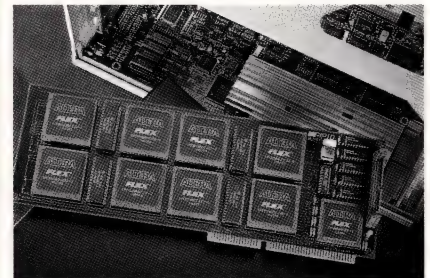
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Designers are able to take advantage of the RIPP 10 by creating logic designs for each EPF81188, using Altera's Max+Plus II development software. Because the entire board is designed with reconfigurable SRAM-based devices, users can store several designs and dynamically reconfigure the board, based on the desired application. Available now, the RIPP 10 sells for \$995. The development software starts at \$1495.

Altera Corp.

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San Jose, CA 95134

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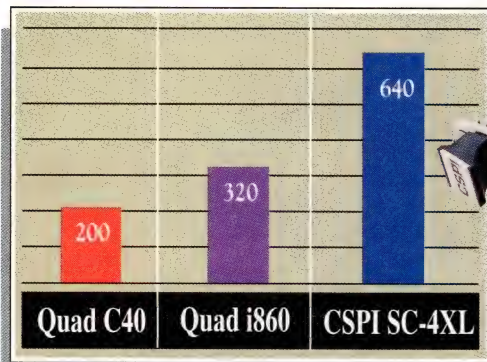
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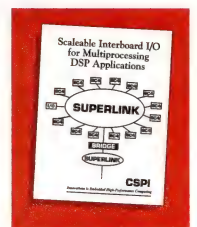
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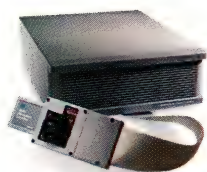
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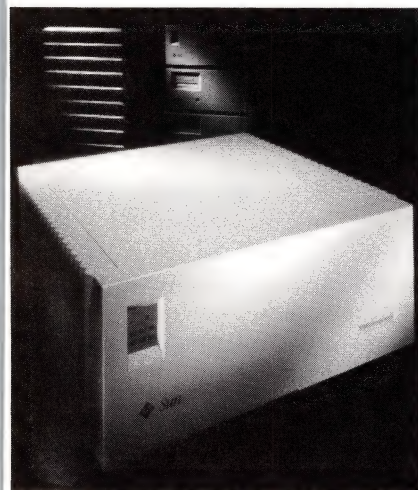
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The problem of limited storage capacity is eliminated by the SparcStorage Array, a mass-storage subsystem that holds up to 30 high-performance 1.05 Gbyte hard-disk drives. RAID levels 0, 1, 0+1, and 5 are supported. The drives in the array are connected by a 20-Mbyte/s fast and wide SCSI-2 link. The connection between the subsystem and



the host is made through a Fibre Channel link. Sun Microsystems, which developed the array, claims that this is the first volume implementation of Fibre Channel. The data-transfer rate of the SparcStorage Array is currently 25 Mbytes/s and a 50-Mbyte/s rate is coming shortly. In addition, a Fibre Channel connection can span up to 2 km.

The drive controller employed in the system is a microSparc microprocessor. Transfer rates are expedited using 4 Mbytes of write cache on the controller. In addition, each drive contains its own local cache memory. A user-friendly software interface permits on-line configuration and tuning of the subsystem.

User maintenance is made easy by the system's modularity. The drives, fans, controller board, and power supply all slide out of the case for replacement or repair. The maximum configuration sells for \$50,900. With about 6 Gbytes of memory, the SparcStorage Array subsystem sells for under \$25,000.

Sun Microsystems Inc.
2550 Garcia Ave.
Mountain View, CA 94043
(415) 960-1300

► CIRCLE 605

▼ SCSI HOST ADAPTER CONNECTS TO PCI BUS

Connecting a peripheral to a PC through a SCSI interface is one way to improve the peripheral's performance, thanks to the increased bandwidth of the interface. But if the SCSI interface is connected to the ISA bus, the bandwidth is limited by the ISA bus' maximum speed. Now the bottleneck of the ISA bus can be averted by using the AHA-2940 host adapter. The host adapter connects to the PCI bus, which handles data-transfer rates up to 133 Mbytes/s. Advanced SCSI features and bus-master DMA data transfers are supported by the adapter.

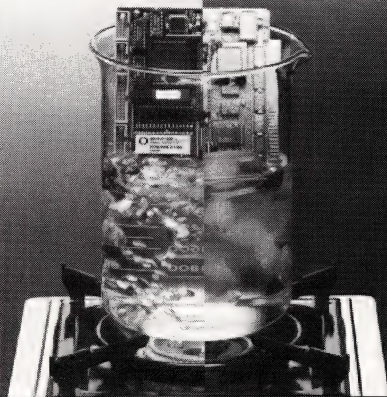
The host-adaptor board is based on a proprietary RISC-based microprocessor called the PhaseEngine. The 10-MIPS processor minimizes the time required to process SCSI commands by automating SCSI phase changes and advanced SCSI features. As a result, the host CPU is free to perform other tasks, improving overall system performance. The programmable PhaseEngine also executes self-contained microcode, which is downloaded by the host CPU at system initialization. This makes it possible to upgrade code with ease. In addition, a 64-byte scratch memory stores configuration information established by the BIOS-resident SCSISelect configuration utility.

The AHA-2940 can connect to 8- or 16-bit SCSI peripherals. It is compatible with all popular operating systems, SCSI-2 and SCSI-3 fast and wide peripherals, and standard application software. As a result, the SCSI bandwidth stands at 20 Mbytes/s for wide 16-bit devices. The SCSISelect utility eliminates the need to set jumpers or terminators while installing the board or adding peripherals. All settings are handled through software. Two versions of the host-adaptor board are available: a bare board that sells for \$195 in OEM quantities, or a \$349 kit that includes the board, installation software for DOS and Windows, cables, manuals, and software drivers.

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SYSTEM DESIGN PRODUCTS

▼ ISOLATE AND EXTEND PCI BUS

The PCIX32 bus-isolation extender makes it possible for 32-bit PCI adapter boards to be added or removed from a PCI system bus without powering down the system. This results in a faster design cycle and easier board testing.

The extender is available in 3.3- and 5-V versions. The height of the extender is just 2 in. and the isolation logic introduces a delay of only 250 ps. A second version is available, the PCIE4, which is a regular extender without the isolation features. The PCIE4 also comes in 3.3- and 5-V versions, and measures 1.5 in. in height. Both PCI-based extenders are currently available. The PCIX32 bus-isolation extender sells for \$355, while the PCIE4 carries its price tag of \$69.

Adex Electronics Inc.
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El Toro, CA 92630
(714) 768-3211
► CIRCLE 107

▼ SOFTWARE SPEEDS UP AUTOCAD

Version 2 of the TurboDLD software-only AutoCAD accelerator is twice as fast as its predecessor. The software adds speed to pans, zooms, and redraws. It supports AutoCAD Release 12 DOS, 3D Studio Release 3, AutoShade 2.0 w/Render Man, and older versions of AutoCAD. Other features include pop-up graphical icon menus, a zoomable spy-glass, pop-up window text, real-time panning, and reconfigurable digitizer buttons. Different software versions are available, ranging from a deluxe version to a light version. A demo can be downloaded from the company's BBS at (603) 432-5193 (filename TURBDEMO.EXE) or from Compuserve's ACAD forum (filename TRBDEM.EXE).

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(800) 729-7420 or
(603) 437-5022
► CIRCLE 608

▼ SINGLE-BOARD COMPUTER HOLDS 68060 CPU

68060-based computer boards are finally starting to flow into the mainstream, with announcements already coming from Motorola and Heurikon. Now Performance Computer has entered the fray with a 68060-based high-performance single-board computer, the PT-VME161, that supports all standard VMEbus data and operating modes, including VME64. The board features 4 to 64 Mbytes of DRAM, a fast SCSI-2 interface with DMA support, and dual asynchronous serial I/O ports. System-status lights and control functions are on the front panel. Optional plug-in daughterboards allow for customization. The PT-VME161 single-board computer will be available sometime in the second half of the year.

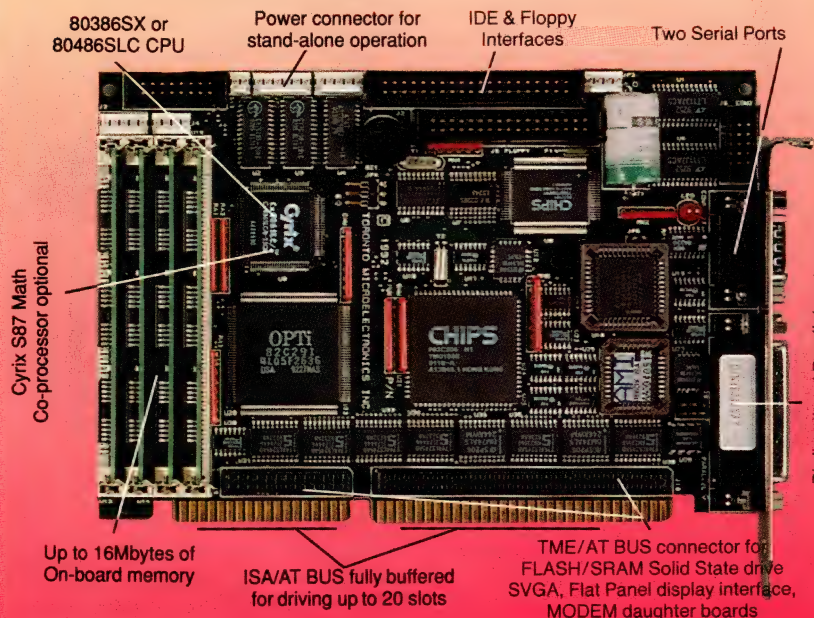
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SVGA/FLAT PANEL DISPLAY INTERFACE



TME's F486SLC	COMPETITOR
✓ 80386SX	Yes
✓ 80486SLC	?
✓ 16/25/33/40Mhz	?
✓ Up to 16 Mbytes of On-board memory	Yes
✓ 64K Write back cache	No
✓ Two serial ports with 10KV ESD Protection	No
✓ One Parallel Port	Yes
✓ Floppy & IDE interface	?
✓ Under 6.5W capability	?
✓ Watch Dog Timer	?
✓ Power Fail Detection	No
✓ Small form factor 4.75" x 7"	?
✓ Optional FLASH/SRAM Solid state drive, Flat panel display, VGA & SVGA interfaces	?
✓ Fully buffered AT BUS for driving up to 20 slots	No

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*Power meter V1.3

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ELECTRONIC DESIGN ■ COMPUTER SYSTEMS SPECIAL EDITORIAL FEATURE ■ APRIL 18, 1994

Pentek Quad 'C40 VME

There are other Quad 'C40 VME boards. They don't come with half the I/O, software, and DSP experience as the Pentek 4270.

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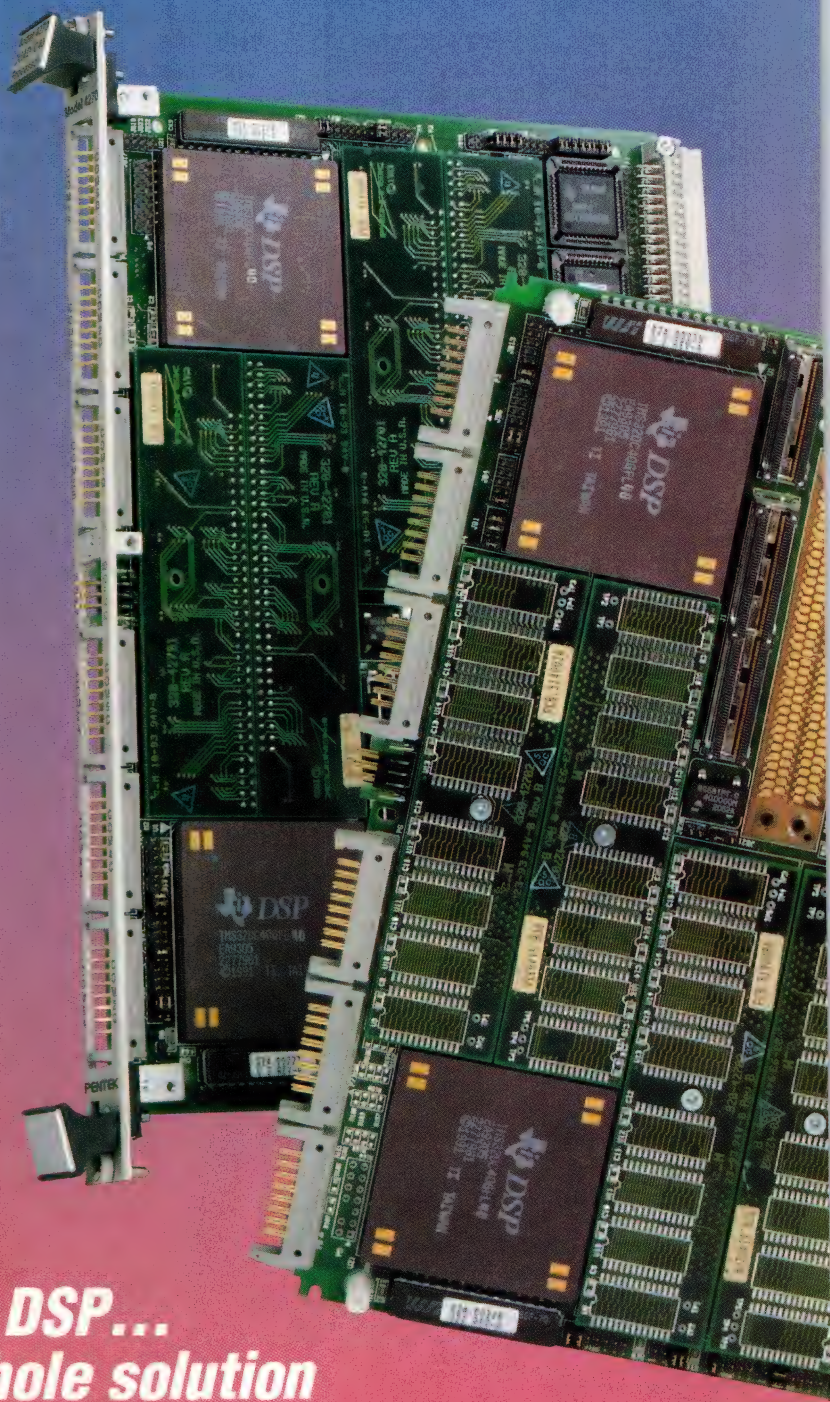
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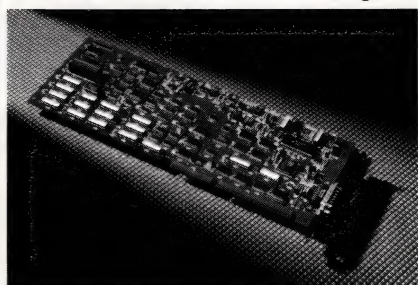
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SYSTEM DESIGN PRODUCTS

▼ LOW-COST FRAME GRABBER WORKS IN REAL TIME

The latest member of the Vision-EZ family of low-cost imaging products is the DT55-LC. The scientific-quality,



square-pixel frame grabber can collect images from video cameras, VCRs, and still-video devices. Four on-board input lookup tables (LUTs) process images in real time as they are acquired. The images are captured with full 640-by-480-square pixel spatial resolution and 256 gray scales.

The bundled Global Lab Acquire software makes it easy to capture, save, and print images in TIFF, PCX, or DT-IRIS formats. The DT55-LC is

aimed at scientific imaging applications, such as microscopy, metrology, and medical imaging. Available now, the DT55-LC sells for \$695, including the Acquire software as well as some diagnostics.

Data Translation Inc.

100 Locke Dr.

Marlboro, MA 01752

(508) 481-3700

► CIRCLE 610

▼ CONNECT PCMCIA TO PCI ON THE DESKTOP

PCMCIA, which began its life as an add-in slot for portable computers, is moving its way onto the desktop. Card designers say that by putting the slots into desktop computers, they needn't design similar peripherals as add-in boards—the same boards can be used for either portable or desktop platforms. To improve the performance of the PCMCIA-based designs, the 82092AA controller lets the cards plug into the system's PCI local bus. Compliant with the PCMCIA 2.01 specification, the

chip assures both interoperability and exchangeability of compatible cards. Designers can implement the 82092AA controller on either a PC motherboard or on an add-in card for Intel 486- and Pentium-based platforms.

The chip supports up to four PCMCIA sockets. It also includes an enhanced local-bus IDE interface that features programmable timing support. The controller is software-compatible with Intel's 365SL PCMCIA controller, thus streamlining the design. It's packaged in a 208-pin plastic quad flat pack. A design kit is available that includes an 82092AA-based PCI add-in card, drive-bay electronics, board-development schematics, and software. The controller sells for \$19 in quantities of 10,000.

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► CIRCLE 611

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▼ LOW-COST X-TERMINAL FEATURES DUAL DISPLAYS

The low-cost XP100D dual-display color X-terminal is designed for financial-industry, dispatch monitoring, and process-control applications. Completely adhering to the X-Window system standards, the platform combines a RISC CPU with proven software to deliver a performance rating of 1.41 Xmarks. The XP100D comes in a low-profile pizza-box package with no fan, making it suitable for office environments. The XP100D is a lower-cost replacement for dual-display workstations. The logic unit sells for \$4695. Two display options are currently available—two 17-in. color displays for \$2850, or two 19-in. color displays for \$4250. The company's XpressWare X-server software ships with the X-terminal.

Tektronix Inc.
P.O. Box 500
Beaverton, OR 97077
(800) 225-5434
► CIRCLE 612

▼ COLOR TOUCH-SCREEN LCD RUNS FROM A PC

Using the VAMP II (Video Analog Monitor Panel) flat-panel system, a 262,000-color TFT LCD and touch screen can be driven directly from a PC. The compact unit (11.5 by 8.5 by 3 in.) plugs directly into a standard VGA output. The large color range and 640-by-480-pixel resolution suit the display for such graphics-intensive applications as presentations, multimedia, or sophisticated machine control. The optional resistive touch screen communicates with the PC through an RS-232 cable. It also comes with a NEMA-rated bezel. In addition, capacitive and infrared touch screens are available. The complete system consumes less than 25 W. Available from stock, the VAMP II flat-panel display system costs \$3995 in OEM quantities.

Computer Dynamics Sales
107 S. Main St.
Greer, SC 29650
(803) 877-8700
► CIRCLE 613

▼ OCR SOFTWARE FOR THE MAC COSTS UNDER \$100

Macintosh users can get high-performance optical character recognition (OCR) for just \$99. Version 2.0 of the TextBridge OCR system offers a unique architecture that applies software algorithms to different elements of the recognition process. Lexifier, for example, advances the concept of contextual interpretation to improve the accuracy for words and other character patterns, such as social-security or telephone numbers. Using artificial-intelligence techniques, TextBridge learns as it reads, taking information gathered from "clean" sections of text to help interpret hard-to-read areas. A word verifier lets users view, confirm, and correct words while the recognition is in process. Foreign languages are also supported.

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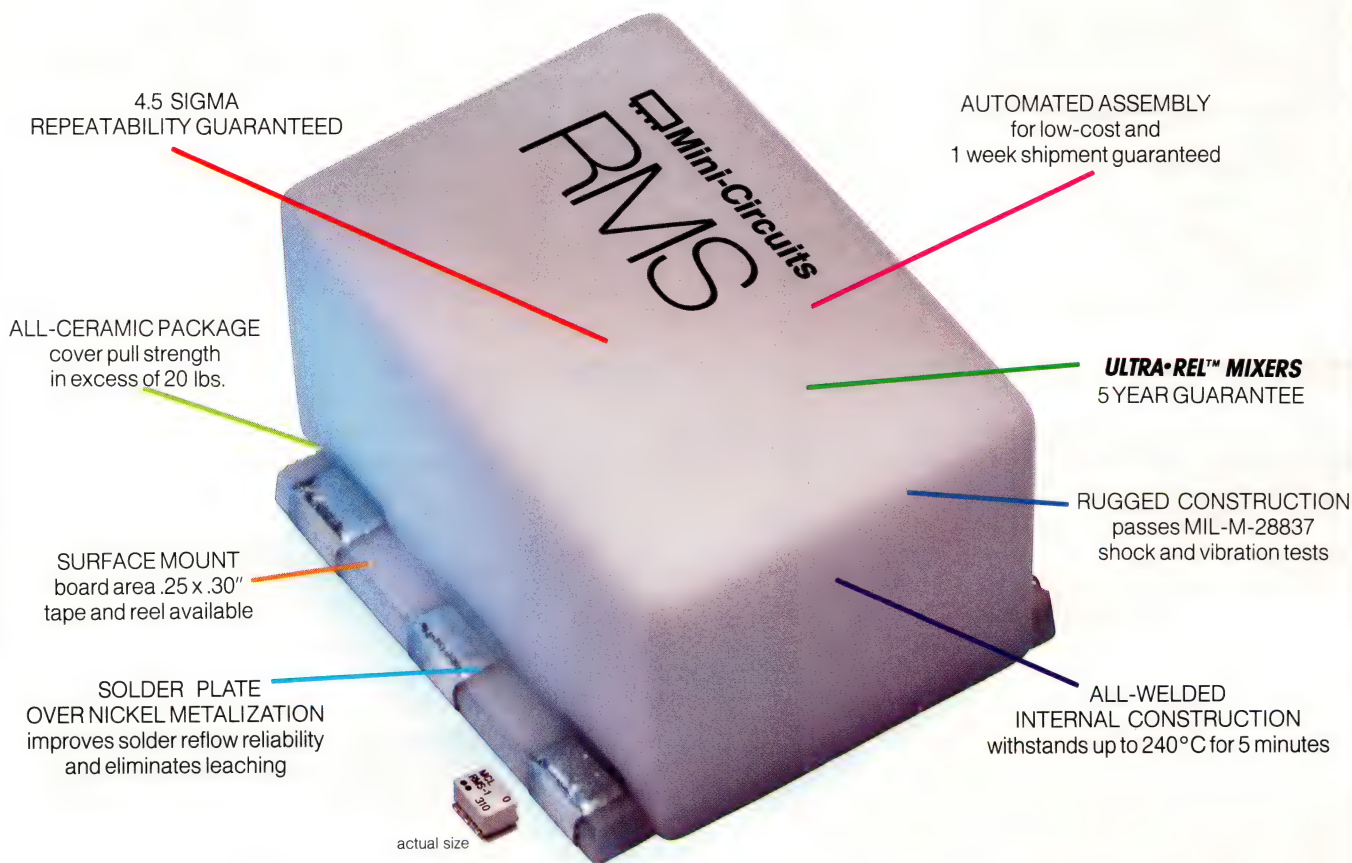
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CUSTOMERS CAN CHOOSE READY-TO-USE DESIGNS, COMPONENTS, AND SOFTWARE FOR THEIR UPCS SYSTEMS.

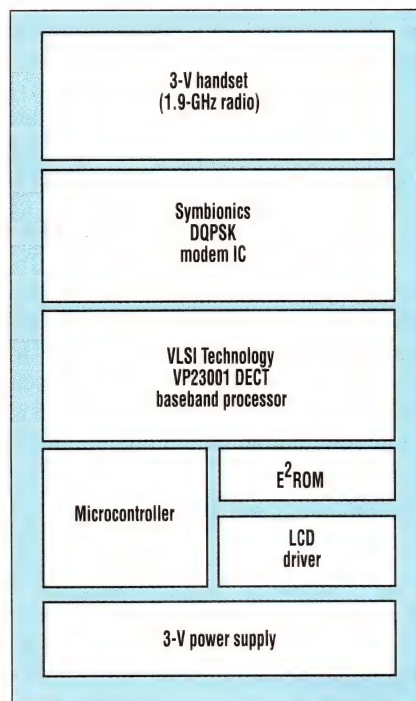
PETER FLETCHER

Most designers find that time-to-market holds the key to success today. With that in mind, those who develop cordless PBX systems conforming with the unlicensed personal-communications system (UPCS) standards may be interested in a package of designs, components, and software aimed at giving them a head start against their competition.

The UPCS "development pack" consists of a set of specimen designs for a 1.9-GHz digital dual-conversion superheterodyne radio transceiver; a set of chips or VHDL sources to make a modulator and demodulator; specimens and design rules for pc-board layouts, and specially developed software modules that can be adapted for use with standard microcontrollers. Included are schematics, bills of materials, and an offer of development assistance. Packs are available for all of the subsystems that make up a cordless PBX system, including a pocket telephone, fixed radio heads, and a combined PBX line-card interface and radio-head cluster controller that's adaptable to existing systems.

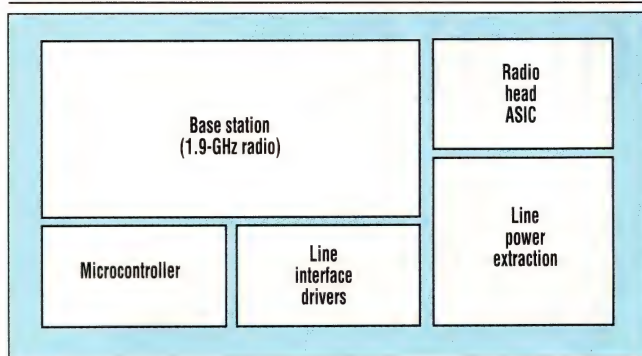
The package, offered by Symbionics Ltd., Cambridge, U.K., has produced an enhanced version of the time-division, multiple-access (TDMA) digital European cordless telecommunications (DECT) technology. The company believes that DECT will be adopted by the Telecommunications Industry Association's TR-41.6 working group as a basis for a UPCS interoperability specifications scheduled for publication this fall. Symbionics also claims that its enhanced DECT technology will meet all FCC requirements for coexistence with other services using frequencies allocated for UPCS between 1.890 and 1.930 GHz.

Symbionics' design pack for the en-

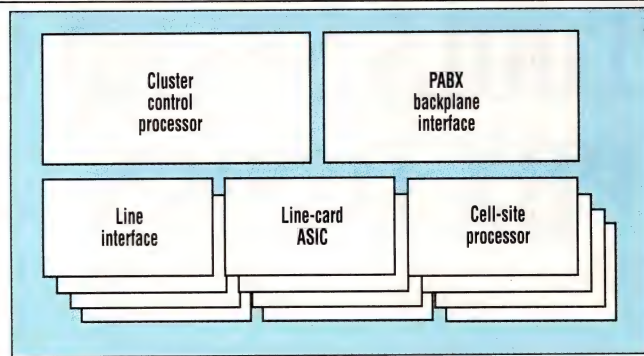


1. THE ORIGINAL DECT technology used Gaussian phase-shift-keying. Symbionics' enhanced version instead employs differential quadrature phase-shift-keying to improve modulation efficiency and meet adjacent-channel interference limits.

PACKAGED CORDLESS PBX SOLUTION



2. THE DESIGN FOR the remote radio heads makes it possible to use lower-cost filters and other frequency-dependent components.



3. BECAUSE line-interface cards must be system-specific, the design covers only that part needed to drive the radio infrastructure.

hanced DECT technology could save up to five man-years' design and development time, according to Jeremy Hendy, senior DECT consultant. He goes on to say that the pack takes advantage of a range of low-cost and proven components and software. "Using our technology package, a PBX designer could have a cordless system—including handsets, fixed radio heads, and a PBX line-card interface—ready for production in less than six months," says Hendy. He notes that two years' development of DECT in Europe for cordless telephone and PBX use has engendered a great deal of investment by component manufacturers in chip sets, low-cost SAW filters, and other standard parts.

To make DECT fit within the FCC rules, Symbionics redesigned the radio transceiver. DECT operates at 1.512 Mbits/s and uses a Gaussian phase-shift-keying modulation scheme that produces one symbol per bit. "That works with DECT because it uses 1.7-MHz channel spacing," says Hendy. Although that scheme delivers less than optimum efficiency, he adds, it was chosen several years ago when cost was the prime consideration.

UPCS channel spacing was set at 1.25 MHz, so the original DECT modulation can't meet the adjacent-channel interference limit. Therefore, to meet the limit, and to improve modulation efficiency, Symbionics retained DECT's baseband processing architecture but switched to differential quadrature phase-shift-keying to encode two bits into each symbol (Fig. 1).

"For each symbol, there is a phase shift of either $\pm 45^\circ$ or $\pm 135^\circ$," says Hendy. "That gives four possibilities for each symbol, so the symbol rate falls to

576 ksamples/s, which requires less bandwidth and allows UPCS channel-spacing requirements to be met."

A radio modem was designed to accommodate this new scheme. The modem converts the 1.512-Mbit/s output from a standard DECT baseband processor (Hendy cites VLSI Technology's VP23001) for transmission at 576 ksamples/s modulated at an intermediate frequency for presentation to the transceiver. The design includes filters and analog-to-digital and digital-to-analog converters together with signal-processing logic.

As a development aid, the company plans to make the modem available as a set of three chips, but Hendy says the company won't manufacture them as standard parts. Instead, a licensee will be given VHDL sources for the circuit logic and enough information to produce the modem either as an ASIC cell or as discrete parts.

To go with the radio modem, Symbionics designed a 1.9-GHz dual-conversion superheterodyne receiver with the appropriate analog interfaces. Hendy says the design is very easy to manufacture and offers yields of up to 95%. The company considered non-IF designs but found them unreliable. He explains that dual conversion means separate VCO loops can be used for modulation and channel switching, so an appropriate channel loop bandwidth can be employed for each function. A one-synthesizer solution might cause conflicts between channel switching and modulation.

This approach also allows lower-cost filters and other critical frequency-dependent parts to be used. The FCC has set a very tight carrier-frequency stability requirement: 10 ppm for the portable phones. The sec-

ond demodulation stage makes it possible to recover the carrier frequency by locking lower-cost voltage-controlled crystal oscillators and SAW filters to the base station (Fig. 2).

Hendy says the radio's output and receiver designs are well proven. In fact, they're based on a chip set from Hewlett-Packard that was developed for TDMA operation at 1.9 GHz. The transmitter power amplifier and receiver low-noise amplifier employ discrete components, but may eventually be integrated into a gallium-arsenide microwave monolithic IC (MMIC). "Our design uses a GaAs final output drive, so when GaAs MMICs get cheap enough, that is an easily replaceable block, he says."

The enhanced DECT technology improves performance and, because it can be implemented digitally, also improves integration. Consequently, although UPCS mandates a lower transmit power than the 250-mW peak allowed for DECT, range will be similar or better. Hendy says that 200 m in the open or 70 m inside buildings will be achievable.

The Symbionics' radio is designed to run on 2.7 to 3 V, and is available for manufacture under license. A licensee will be supplied with sample devices for prototyping. Schematics for a suitable GaAs-based power amplifier for the transmitter and a low-noise amplifier for the receiver are included.

The kit will include a sample printed-circuit board and a full technical manual with design rules and recommended layouts. Software to control the radios also is available. The software is based on that used in Symbionics' range of DECT test systems employed by European manufacturers and approvals-test laboratories.



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In addition to mobile telephones and base stations, Symbionics developed low-level software and design recommendations for line-interface cards. These cards can be fitted to a standard PABX to give it cordless capability. Because a line-card design would be specific to a particular manufacturer's system, the company defined only the part of the card that's required to drive the radio infrastructure—generally remote radio heads connected to the PABX by cable (*Fig. 3*). The remote heads can be operated as single units or in clusters.

Hendy notes that unlike the European regulators, the FCC doesn't stipulate the technology that must be employed for UPCS. The only rules are that the system must be digital and it must not interfere with existing users. The relevant frequencies are used for point-to-point microwave links, so the main limitations for UPCS systems are on transmit power, channel spacing, and spurious emissions.

Although the FCC hasn't defined a mandatory standard for UPCS, the agency wants to ensure a measure of interoperability between equipment supplied by different manufacturers, especially for cordless PABX and domestic cordless systems. The responsibility for defining a specification was delegated to the Telecommunications Industry Association, which formed the TR-41.6 Wireless User Premises Equipment Engineering Subcommittee to produce a specification that its members can adopt. □

PRICE AND AVAILABILITY

The enhanced DECT technology and related tools, available now, is being offered together as licensable technology. Fees will be negotiated and based on a customer's specific needs. In general, the licenses will be non-exclusive and take the form of one-time fees, with no royalties involved.

Symbionics Ltd., St. John's Innovation Park, Cowley Rd., Cambridge, CB4 4WS, England; phone: (44) (0)223 421025; fax: (44) (0)223 421031.

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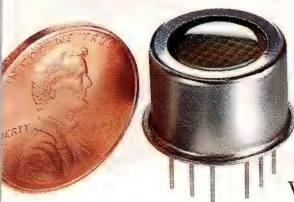
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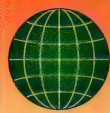
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NEWSLETTER



STANDARDIZED NIMH CELLS TO POWER NOTEBOOK PCs

Following on the heels of its announced plan to introduce standardized nickel-metal-hydride rechargeable-battery packs, Duracell Inc., Bethel, Conn., landed a major design win for a sub-notebook computer application. Compaq Computer Corp., Houston, Texas, will feature Duracell's DR19 and DR31 NiMH packs in its forthcoming Contura Aero family of sub-notebooks, and thereby become the first major computer company to design-in the packs. The DR19 pack will power a 486SX-based monochrome system, while the DR31 pack will be offered as a longer-lasting power option. The packs each deliver up to 40% longer life than comparably sized nickel cadmium batteries, and provide the Contura Aero with up to four and six hours of run time, respectively. Replacement batteries will be available through retail channels and carry suggested prices of \$99 and \$169 for the DR19 and DR31, respectively. *DM*

CIRCLE 941

DEBUG EMBEDDED MULTICOMPUTERS

A system-level debugger for real-time embedded multicomputers enables developers to troubleshoot applications running on multiple processors simultaneously. SuperVision, which works with Race multicomputers from Mercury Computer Systems, Chelmsford, Mass., can debug systems running on one to hundreds of processors. The debugger accesses the run-time environment through Mercury's MC/OS distributed realtime OS, which organizes the multicomputer system through windows that provide visibility of the entire system or subset areas of interest. SuperVision runs on Sun workstations under Solaris 1.1/SunOS 4.1.3. Pricing starts at \$5500 for a single-user license. *SVT*

CIRCLE 942

DEVICE SHUTS DOWN PC DISPLAY

Electric bills can be reduced using the Green Keeper from B&B Electronics, Ottawa, Ill., which automatically shuts down a computer's display. The device is similar to a screen blanker, except that it turns off the power rather than just blank the display—the rest of the computer remains on. It connects in series with the keyboard of a PC—the display is plugged into the Green Keeper. The software, which runs under either DOS or Windows, monitors the computer's activity and shuts off the display after a user-specified period of inactivity. A touch of the keyboard or mouse brings the display back to life. The inactivity period can be set to different intervals for different parts of the day. For example, it could be set to 15 min. during business hours, 1 min. during lunch time, and 1 min. during non-business hours and weekends. Up to nine different time-outs can be set. The Green Keeper costs \$69.95. For more information, call (815) 434-0846. *RN*

CIRCLE 943

HIGH-SPEED PWM CONTROLLER

By employing a biCMOS process and a new voltage-mode architecture, Unitrode Integrated Circuits, of Merrimack, N.H., came up with a highly efficient, high-switching-speed, switching-regulator controller for off-line power supplies. The UCC3570 starts up on just 85 μ A of quiescent current and runs at 500 kHz on just 1 mA. However it can charge the gate capacitance of a MOSFET with 1 A pulses of PWM. The IC incorporates a unique technique that the company calls voltage-feedforward, which provides fast and accurate response to wide variations in line voltage without the sensitivity to noise inherent in other approaches.

The UCC3570 offers all the advantages of voltage mode control (over current mode), such as providing stable PWM operation under light loads and minimum input voltage. Moreover, slope compensation is not required and the circuit contains only one feedback loop instead of two. In voltage-feedforward, the slope of the oscillator ramp is proportional to the input voltage so that input variations are passed directly to the modulator—essentially bypassing the output filter and error amplifier. The circuit responds instantly (within one clock cycle) to input-line voltage changes, greatly simplifying loop-feedback compensation. Fast current limiting allows the IC to latch the supply off after a programmable number of repetitive faults has occurred. It allows the supply to ride through a temporary overload while still shutting down in the event of a permanent fault. The IC is designed to take isolated dc feedback from the output via an optocoupler. The UCC3570 comes in 14-pin DIPs and SOICs and a 20-pin PLCC. Pricing starts at \$2.10 each in 1000's. *FG*

CIRCLE 944

Edited by Clifford Meth

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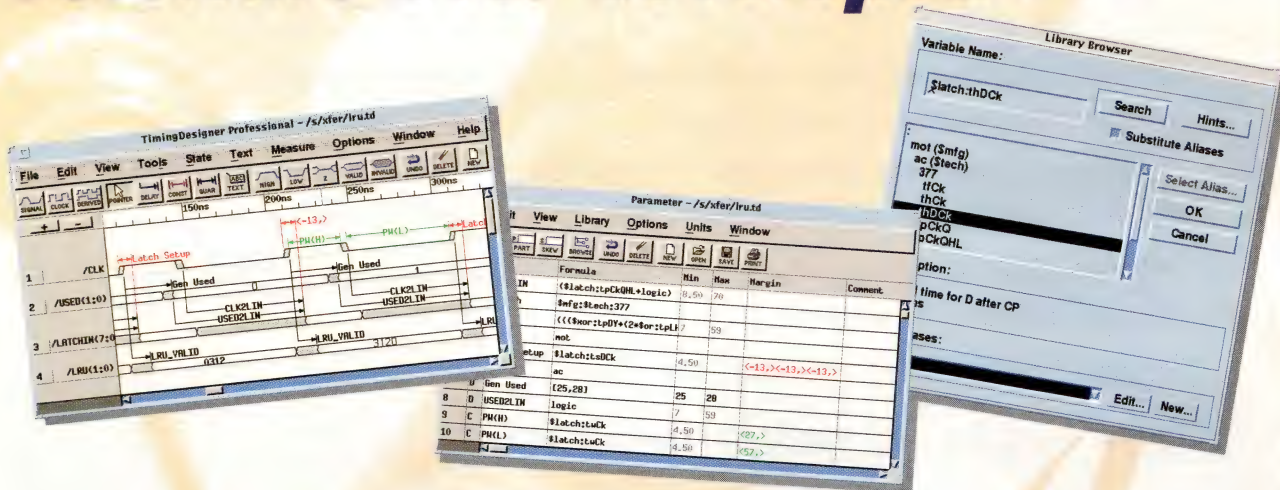
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READER SERVICE 188

NEW PRODUCTS

INSTRUMENTS

TEST SOFTWARE HANDLES INSTRUMENTS OR BOARDS

TestPoint is a multitasking, object-oriented software package that helps users create test, measurement, and data acquisition applications in Windows without conventional programming techniques. The software supports more than 70 popular instruments and plug-in boards, with IEEE-488, RS-232, and RS-485 capabilities. Users can develop custom interfaces, test routines, and report files; process and display data; and exchange information with other Windows applications. Users have full access to external subroutines written in any conventional languages that can create a Windows dynamic link library. The package runs on IBM-compatible AT, 386, and 486 computers with Windows 3.1 or later. TestPoint costs \$995 and is available from stock. JN

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (216) 248-0400. **CIRCLE 670**

TEST CLIPS CONNECT TO 0.3-MM PGFP PACKAGES

A family of miniature test clips allow test engineers who design microprocessor-based systems to clip onto soldered-on PQFP leads with pitches as small as 0.3 mm. The clips incorporate grabbers that can be connected to the board under test when it's active. The grabbers' ultra-thin size allows an unlimited number of clips to be mounted side-by-side for simultaneous testing of multiple pins. Also included are two test probes than can be used on an active chip. The probes work with various logic analyzers and oscilloscopes. The test clips, which cost from \$2.40 to \$50 in single-unit quantities, are available immediately. JN

Emulation Technology Inc., 2344 Walsh Ave., Bldg. F, Santa Clara, CA 95051; (408) 982-0664.

CIRCLE 671

CAD SOFTWARE LOCATES INVISIBLE IC CONDUCTORS

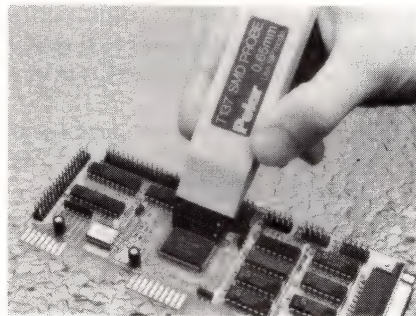
The IDS CAD Layout Overlay accurately locates invisible buried conductors for precision focused ion-beam (FIB) milling. It also enhances e-beam probing by distinguishing conductors that may be difficult to

see due to global or local field effect, planarization, or think passivation. The software superimposes an outline form of the top-metal CAD layers onto the FIB or e-beam image. The operator can then perform an accurate local overlay alignment using the visible surface topography of the top layer. The process takes only a few seconds. The IDS CAD Layout Overlay comes in two configurations. The first is as part of the Invisible Conductor Location Tool for the P2X probe-point-cutting FIB system. That tool costs \$85,000. Users of Schlumberger e-beam systems who already own Layout Tool can buy the system for \$35,000. Delivery is in 30 days. JN

Schlumberger Technologies, ATE Div., 1601 Technology Dr., San Jose, CA 95110-1397; (408) 437-5091. **CIRCLE 672**

32-PIN PROBES AIM AT FINE-PITCH SMT DEVICES

The T-Series handheld high-density probes allow for fast connections to test fine-pitch surface-mount compo-



nents. The probes, the T-Series-137 and -138, offer a row of 32 pins for 0.025-in. or 0.65-mm pitch devices. Thus, users can access devices packed too densely for conventional IC clips, eliminating the need to probe each pin individually. The units work with the company's portable fault locator instruments employing analog signature analysis techniques, which find the cause of a failure on a pc board by checking each component in turn. An innovative comb-shaped guide facilitates probe alignment with an IC's legs. The test pins themselves are spring-loaded for positive contact. The T-Series probes cost \$695. JN

Polar Instruments Inc., 522 Sprague Valley Dr., Sumas, WA 98295; (206) 599-1430. **CIRCLE 673**

PAY-PER-USE TESTER MINIMIZES CAPITAL COSTS

The HP 3070 pay-per-use system offers electronics manufacturers the ability to match their testing costs to their production needs. Users can obtain a fully configured combination tester for about the price of an HP 3072 unpowered-test system. For unpowered opens testing, users pay no additional cost. Digital in-circuit and combinatorial testing is charged on a pay-per-use basis. Charges are made with a "test-credit button," which customers buy and insert into a tamper-proof lock box on the tester. As the tester runs the higher levels of tests, it debits the test credits stored in the button at rates that depend on the test being run. The system can be upgraded to an HP 3073 or HP 3075. All hardware costs and 50% of credit-button costs accrue as equity toward an upgrade. Prices depend on node count, with a 1300-node system going for \$132,000. Delivery is in eight to twelve weeks. JN

Hewlett-Packard Co., Direct Marketing Org., P. O. Box 58059, MS51 L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844, ext. 8024. **CIRCLE 674**

TESTABILITY TOOL DOES ANALYSIS AND SYNTHESIS

DFTAdvisor is a test synthesis tool for minimizing test problems in complex ASICs, ICs, and MCMs. The software inserts test logic that improves testability and properly prepares designs for automatic-test-pattern generation. As a result, users can identify test problems and correct them before the test-generation phase. After the problems are identified, DFTAdvisor allows designers to insert scan and test logic structures to improve testability. The resulting design is passed through a comprehensive rule checker. DFTAdvisor can be used in a tightly integrated design environment with other Mentor Graphics products, or as a point tool in other design flows. DFTAdvisor is available immediately on HP 700 and Sun Sparc platforms. Prices start at \$20,000 for a floating license. JN

Mentor Graphics Corp., 8005 S.W. Boeckman Rd., Wilsonville, OR 97070-7777; (503) 685-7000.

CIRCLE 675

ARB FEATURES 12-BIT RESOLUTION, FLEXIBLE TRIGGERING MODES

The Model 2650 arbitrary waveform generator offers a 12-bit vertical resolution with a 50-Msample/s sampling rate. The instrument is available in one- or two-channel versions, with a horizontal resolution of up to 256 kpoints/channel.

Flexible triggering options include continuous, triggered, gated, or burst mode. Also, users can select from four trigger sources: an internal clock, an external input, a manual trigger, or use of the second channel. In burst mode, the unit will supply from 2 to 999,999 waveform selections. For added flexibility, an external AM signal can be used to modify the output waveform's amplitude.

Voltage output ranges from 15 mV to 15 V pk-pk, with a rise time of less than or equal to 15 ns. In the two-channel version, each channel has its own amplitude, offset, and timing settings. Standard waveform memory is 64 kpoints/channel.

The 2650 is compatible with National Instruments' LabWindows and Rapid Systems' R4 drivers. All parameters, modes, and functions are programmable and fully compatible with IEEE-488.2 and the Stan-



dard Commands for Programmable Instruments.

Waveforms can be created from the front panel using point and line-segment entry, or produced mathematically on a personal computer and downloaded to the instrument. Waveform points may also be directly transferred from a computer graphics program. Real-world signals can also be captured on a digital oscilloscope and sent to the instrument for generation.

A one-channel 2650 costs \$3995, and a two-channel version costs \$5990. The expanded memory option is \$495 per channel. Delivery is in two weeks.

Analogue Corp., 8 Centennial Dr., Peabody, MA 01960; (508) 977-3000. CIRCLE 676

■ JOHN NOVELLINO

26.5-GHz TEST RECEIVER BOASTS LOW NOISE LEVEL

A triple-conversion heterodyne receiver, a spectrum analyzer with color display, and a scalar network ana-



lyzer are integrated into a single system to create the ESMI test receiver. The receiver, which is completely CISPR-compliant, aims at electromagnetic-compatibility measurements from 20 Hz to 26.5 GHz (and to

110 GHz with an optional external mixer). Noise level is less than -145 dBm (-160 dBm using the internal 10-dB preamplifier), and intermodulation-free dynamic range is more than 100 dB. Phase noise at a 1-kHz offset is 105 dBc/Hz at 100 MHz, 102 dBc/Hz at 5 GHz, 90 dBc/Hz at 20 GHz, and 88 dBc/Hz at 26 GHz. With 384 bandwidths between 6 Hz and 3 MHz, users can specify precise frequencies for channel monitoring and demodulation. The unit has four display memories, an HP-GL plotter output, a Centronics parallel port, and IEEE-488 and RS-232C interfaces. ESMI prices start at \$98,000, with delivery in 14 weeks. JN

Tektronix Inc., Test & Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200. CIRCLE 677

MULTI-CHANNEL CARDS DO ANTI-ALIAS FILTERING

The Model AAF-xx series of multi-channel, low-pass filter cards are well-suited for anti-aliasing applications in PC-based data acquisition systems. The series includes six models of two, four, or eight channels, with one or two stages of five-pole filtering. Each externally mounted card accepts ± 10 , ± 5 , ± 2.5 , and ± 1.25 V inputs. Each channel has software programmable gains of 1, 2, 4, and 8, as well as two-stage cascaded filtering. Cutoff frequencies of 1 Hz to 50 kHz are selectable by a combination of an on-board DIP switch and a software programmable 16-bit counter from an external analog-to-digital card. The cards come with set-up, calibration, and sample programs and with software drivers for popular Access I/O a-d cards. Prices run from \$695 to \$1675 with delivery from stock to one week. JN

Access I/O Products, 9400 Activity Rd., San Diego, CA 92126; (800) 326-1649. CIRCLE 678

HIGH-SPEED IC TESTER HANDLES MEMORIES ALSO

Memory test capability is now available on the HP 83000 Model F660 IC tester. The 660-MHz, ± 50 -ps system handles stand-alone static memories to more than 200 MHz and ICs embedded with static RAM cell arrays or multi-die memory modules. For true topological fault diagnosis, the system provides X-X and X-Y descrambling and algorithmic data-inversion support. In addition to the F660's logic analysis tools—such as timing diagrams, error maps, and state lists—a full-fledged bit map is available to display the true topological structure of memories with up to 4 million address bits. Specifications include an address size of up to 16X, 16Y, a data width of up to 512 bits per port, and as many as 16 independently selectable APG ports per test. A typical system for high-speed RAM testing costs about \$650,000. Delivery is in eight weeks. JN

Hewlett-Packard Co., Direct Marketing Org., P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 752-0900, ext. 8074. CIRCLE 679

WORLD'S SMALLEST MOST ACCURATE QUAD 12-BIT V_{OUT} DAC

Cut Space, Eliminate Costly Trims!

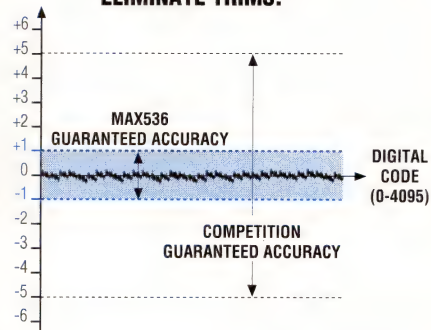
The MAX536/MAX537 is ideal for servo-control, offset/gain-adjust, and other applications where high precision and small form-factor are critical. 12-bit monotonicity, $\pm 1/2$ LSB relative accuracy, and ± 1 LSB Total Unadjusted Error* (MAX536) are guaranteed with no zero- or full-scale adjustments. The four DACs can be updated either independently or simultaneously via a single command register, and the serial interface is fully compatible with SPI™, QSPI™, and MicroWire™.

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- ◆ **± 5 V Supply Operation (MAX537)**
- ◆ **Low-Noise Precision Output Buffers On-Chip**
- ◆ **Parallel Versions Also Available (MAX526/MAX527)**

IMPROVE ACCURACY 5 TIMES, ELIMINATE TRIMS!



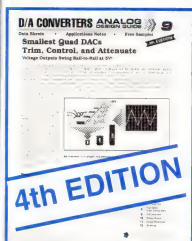
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*Total Unadjusted Error (TUE) = Sum of Linearity, Offset and Gain Errors.

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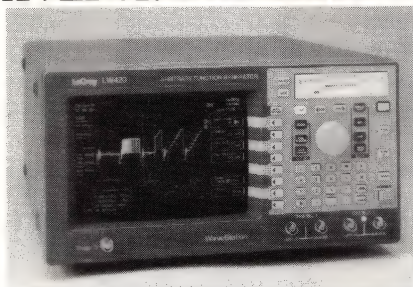
READER SERVICE 179

EASY-TO-USE ARB BOASTS 100-PS RESOLUTION, LONG WAVEFORM MEMORY

The WaveStation 400 series arbitrary waveform generators feature 100-ps feature-placement resolution, a 400-MHz maximum clock rate, and 256-kbytes of waveform memory per channel. In addition, state-of-the-art digital-signal-processing technology and precision reconstruction filtering techniques make it easy to enter waveforms in a variety of ways.

The LW410 (one channel) and LW420 (two channels) have a 9-in. amber CRT display, so users can immediately view results. Vertical resolution is 8 bits and a 1-Mbyte waveform memory is optional. The units' timebase accuracy is 3 ppm with a stability of 1 ppm/yr. Single side-band phase noise is less than -120 dBc/Hz at 10 kHz from a 10-MHz carrier.

Waveforms can be created by using built-in standard or custom waveform libraries, the unit's equation editor, or signals transferred directly from a digital scope, or from one of several compatible software packages. The WaveStation determines the optimal clock rate and filtering characteristics needed and generates the waveform automati-



cally. The instrument employs a smoothing technique that minimizes the discontinuities often created when waveforms are modified in an arbitrary generator.

Waveforms can be transferred from most popular digital scopes over a GPIB cable. No personal computer or other controller is required. Also, a 3.5-in. floppy drive is standard so users can transfer waveforms from a PC, workstation, or digital scope.

The LW410 costs \$13,945, and the LW420 is \$18,950. The 1-Mbyte memory option is \$3495 for the LW410 and \$4995 for the LW420. Delivery is within six to eight weeks.

LeCroy Corp., 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 425-2000.

CIRCLE 680

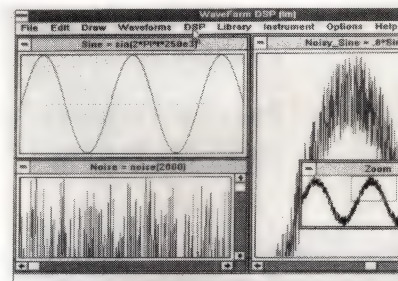
■ JOHN NOVELLINO

packages. The Advanced Software Option package extends support to C and Pascal under DOS and all Windows programming languages. The boards feature single- and dual-channel DMA and a 1-kword FIFO buffer. Both features help avoid gaps in the collected data when operating for extended periods at fast acquisition speeds over multiple channels. The FIFO buffer also compensates for Windows-related interrupt latencies. A variety of triggering choices allows various combinations of pre- and post-trigger acquisition options. The DAS-1801HC accepts 0-to-+5-V or ± 5 -V inputs, and the DAS-1802HC handles 10-V swings. The boards cost \$1299, and the advanced software option is priced at \$99. Both are available from stock. JN

Keithley Metrabyte, 440 Myles Standish Blvd., Taunton, MS 02780; (800) 348-0033. CIRCLE 682

WINDOWS SOFTWARE CREATES WAVESHAPES

Waveform DSP is a Windows-based software tool for creating, editing, and analyzing waveshapes. The software allows users to generate waveforms using any combination of drawing, math expressions, digital scope downloading, insertions from a library, or data values from other



OMEGA

Model SWD-WF DSP
Software Tool Kit for Designing & Processing Waveshapes

applications, such as Microsoft Excel. A digital-signal-processing engine, based on array mathematics, handles most complex signal creation and analysis needs. The software can output the waveshapes it creates through an arbitrary waveform generator. Waveform DSP costs \$895. JN

Omega Engineering Inc., 1 Omega Dr., P.O. Box 4047, Stanford, CT 06907-4047; (203) 359-1660.

CIRCLE 683

DSP ADDS POWER TO 8-CHANNEL I/O BOARD

The Sig32C-8 uses the AT&T DSP32C to combine 32-bit floating-point digital signal processing with eight channels of analog I/O capability on a 7.5-in PC plug-in board. Each channel contains 16-bit sigma-delta analog-to-digital and digital-to-analog converters and programmable input gain, output attenuation, and sampling rate (to 48 kHz). The board works with the company's Hypersignal-Macro and Hypersignal-Acoustic software, and the new Windows-based DSPower program, which offers a block-diagram user interface and source-code generation. The hardware-software combination offers DSP-based instrumentation, waveform visualization and display, automation of development and test

sequences, and many other DSP tools. The combined Sig32C-8, Hypersignal-Macro, and DSPower package costs \$3995. JN

Signalogic, 9704 Skillman No. 111, Dallas, TX 75243; (214) 343-0069. CIRCLE 681

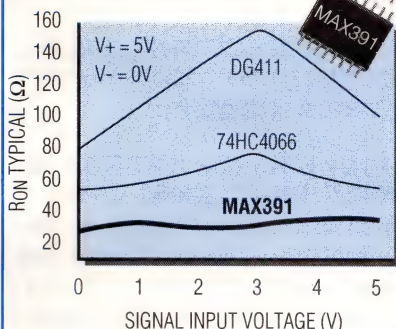
FAST I/O BOARDS HANDLE HIGH CHANNEL COUNTS

The DAS-1800HC Series analog and digital I/O boards feature 12-bit resolution, up to 333-ksample/s acquisition speeds (312.5 ksamples/s in multichannel operation), and 64 single-ended or 32 differential analog inputs. The standard software supplied includes installation, configuration, and calibration utilities; DOS-based menu-driven control panels; a function-call driver, and an external driver for use with application

THE ONLY +5V CMOS SWITCHES WITH GUARANTEED 6Ω RON FLATNESS!

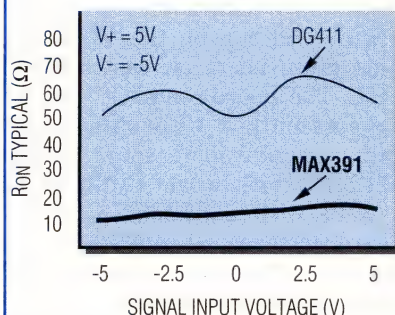
2Ω Max. Channel-to-Channel Matching

**RON vs. SIGNAL VOLTAGE
(SINGLE SUPPLY)**



The new MAX391/MAX392/ MAX393 quad CMOS SPST switches are fully specified for +5V and ±5V operation. With 2Ω max RON matching, 6Ω max RON flatness, and 0.5μW power consumption, these switches are ideal for low-voltage, high-accuracy data acquisition and audio signal routing applications. All switches are pin-compatible with industry-standard devices and operate over a wide +3V to +15V or ±3V to ±8V supply range.

**RON vs. SIGNAL VOLTAGE
(DUAL SUPPLIES)**



Low-Voltage Switches Offer Improved Parameters!

Device*	RON (Ω) max	ΔRON Match (Ω) max	RON Flatness (Ω) max	Leakage (pA) max	Charge Injection (pC) max	ton (ns) max	toff (ns) max
±5V Operation							
MAX391 Quad, SPST, NO	30	2	4	100	5	130	75
MAX392 Quad, SPST, NC	30	2	4	100	5	130	75
MAX393 Quad, SPST, 2-NO,2-NC	30	2	4	100	5	130	75
+5V Operation							
MAX391 Quad, SPST, NO	60	2	6	100	5	130	50
MAX392 Quad, SPST, NC	60	2	6	100	5	130	50
MAX393 Quad, SPST, 2-NO,2-NC	60	2	6	100	5	130	50

*NO = Normally Open, NC = Normally Closed

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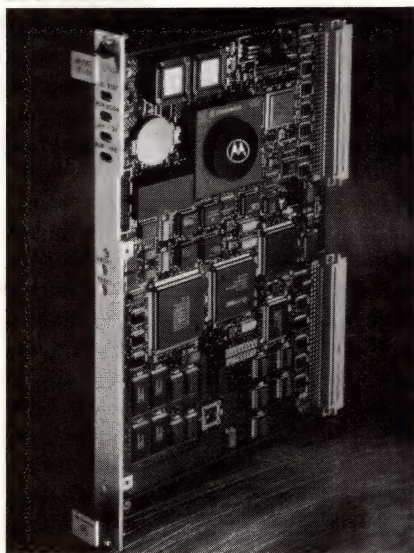
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VME SBC OFFERS 3X IMPROVEMENT OVER PREVIOUS GENERATION

The MVME177 VMEbus board, based on Motorola's latest 32-bit processor, is suited for scientific, industrial, and high-end control applications. The single-board computer (SBC) maintains compatibility with earlier boards and, as a result, all of the software and operating systems developed for existing Motorola VME boards will run on the MVME177. This gives users an easy upgrade path. The board supplies complete support for the VMEbus D64 specification, thereby increasing the VMEbus bandwidth to over 50 Mbytes/s.

Built with a 50-MHz CPU, the board achieves 80 MIPS—a three-times improvement over 68040-based boards. Its on-board features include an Ethernet interface with 32-bit local-bus DMA, an 8-bit SCSI-2 interface, a user-definable mezzanine architecture, four serial ports, and a parallel port. Memory expansion up to 256 Mbytes is possible by replacing the existing memory mezzanine board with a new module, or by adding a second module. The use of on-board flash memory (4 Mbytes)



allows remote downloading of firmware. The four-way interleaved DRAM offers error correction. The board also has room for 128 kbytes of battery-backed SRAM.

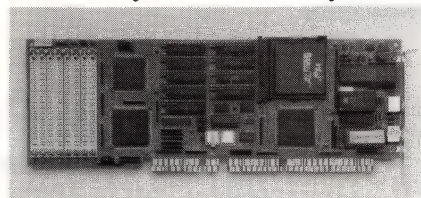
The MVME177 is currently sampling. Production will begin in June, with prices starting at \$4995.

Motorola Inc., 2900 South Diablo Way, Tempe, AZ 85282; (602) 438-3287. **CIRCLE 684**

■ RICHARD NASS

EISA SBC HOLDS 486 OR OVERDRIVE CPU

The 486ES single-board computer, designed with an Intel 486DX or OverDrive CPU, fits into an EISA form factor. Accepting up to eight SIMMs, the board can hold 128 Mbytes of parity-checked DRAM and 1 Mbyte of secondary cache



memory. An on-board real-time clock with battery backup offers a projected life expectancy of ten years. Connectors are supplied for external reset, speaker, mouse, and keyboard ports.

The 486ES can be used in any passive backplane that's compatible

with the PCXI EISA Passive-Backplane Standard. The card occupies "slot 0" in the backplane and supports up to six EISA master boards. Additional slots can handle EISA and ISA slaves. Available now, the 486ES is priced at \$875 for a 33-MHz model with 256 kbytes of cache memory and no DRAM. RN

Interlogic Industries, 85 Marcus Dr., Melville, NY 11747; (516) 420-8111. **CIRCLE 685**

MILITARY VME BOARD SUITS MULTIPROCESSING

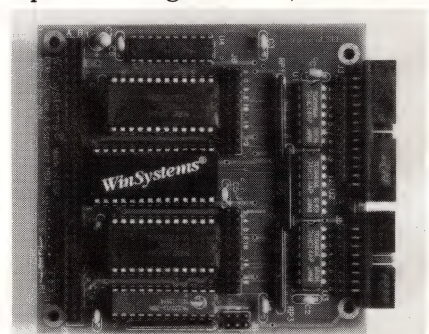
The Advanced Vector Processor (AVP) is a militarized version of the SuperCard-2XL DSP multiprocessor board. The expandable AVP can be programmed easily, and supplies real-time DSP functions tailored to military applications, including sonar, radar, communications, and image processing.

In a single-slot VMEbus form factor, the board's modular arrangement suits it for embedded applications, as well. Performance increases linearly as nodes are added, ranging from 132 MFLOPS in a single node, to 1056 MFLOPS using the maximum eight nodes. Real-time multitasking and multiprocessing is supported. A complete Ada environment is also available. Single quantities of the AVP multiprocessor board, which are available now, sell for \$54,700. Large-volume discounts apply. RN

CSPI, 40 Linnell Circle, Billerica, MA 01821; (800) 325-3110 or (617) 272-6020. **CIRCLE 686**

MODULE EASES EMBEDDED TIMING PROBLEMS

Designed to solve the common timing problems typically found in embedded designs, the PMC-CTC low-cost counter-timer has six independent 16-bit channels, which are all capable of frequency-event counting from dc to 10 MHz. The module, which is built to the PC/104 form factor, can also handle pulse-marker or square-wave generation, time-inter-



val measurements, and single-shot simulation. All six independent channels have a buffered clock, gate, and output available to the user. The individual channels can be cascaded for longer sequences to supply maximum configuration flexibility. Designed with CMOS logic devices, the board consumes just 5 mW and operates in the -40° to +85°C temperature range, making it suitable for harsh and industrial environments. The PMC-CTC module is priced at \$125. Delivery is from stock to two weeks. RN

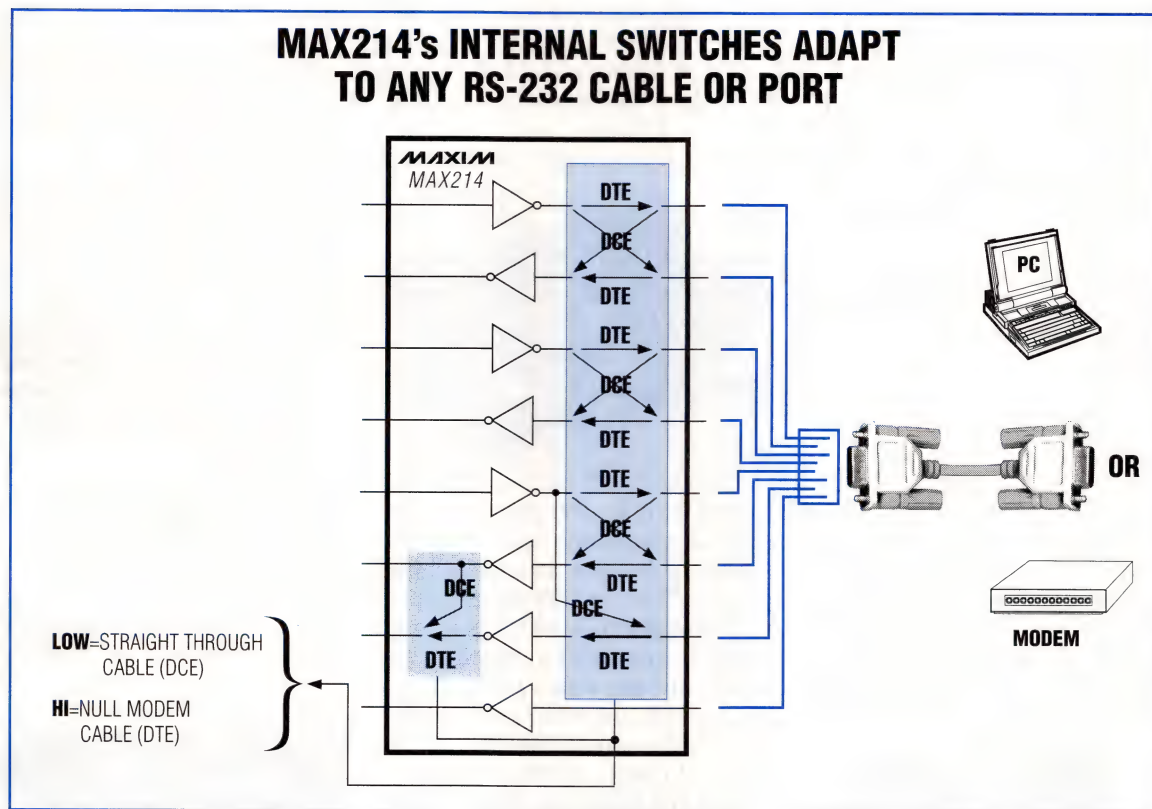
WinSystems Inc., 715 Stadium Dr., Arlington, Texas 76011; (817) 274-7553. **CIRCLE 687**

RS-232 IC ELIMINATES MULTIPLE CABLES AND MAKES NULL MODEMS OBSOLETE

One IC connects directly with both DTE and DCE ports!

Maxim's new MAX214 changes from a DTE port to a DCE port with the flick of a switch, eliminating the need for null modem cables. The +5V powered MAX214 meets EIA/TIA-232 specifications, is guaranteed to run at data rates up to 120kbps, and has a low power shutdown mode that reduces supply current to 20µA.

MAX214's INTERNAL SWITCHES ADAPT TO ANY RS-232 CABLE OR PORT

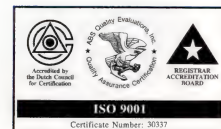


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NEW PRODUCTS

COMPUTER BOARDS

16-BIT SOUND CARD HAS TWO CD-ROM INTERFACES

With two CD-ROM interfaces that support both Sony and Mitsumi drives, the MV-16 eliminates the need for additional adapters and also produces 16-bit digitized audio playback. The card's integrated 4-W amplifier drives headphones or a pair of speakers and contains a volume control. Input-antialias and output-smoothing filters result in high-quality stereo sound.

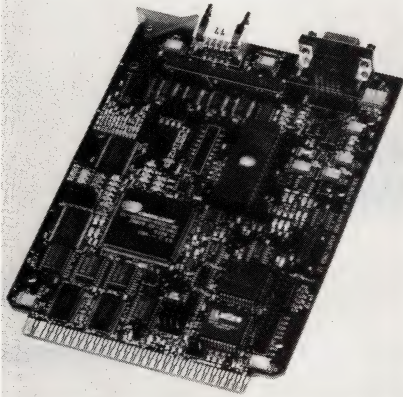
The microphone input contains an automatic gain-control amplifier. A MIDI interface accepts a MIDI synthesizer or other MIDI-compatible musical device. The MV-16 board maintains compatibility with SoundBlaster and AdLib sound boards. A Windows-based software installation utility automatically configures the card. RN

Ocean Information Systems Inc.,
688 Arrow Grand Circle, Covina,
CA 91722; (800) 325-2496.

CIRCLE 688

STD 32 SVGA BOARD SUPPORTS FLAT PANELS

Super VGA (SVGA) capability and flat-panel display support are available to industrial STD 32 computers using the ZT 8982 interface board. The board is based on the Cirrus Logic GD6440 video controller, which supplies enhancements to the Windows operating environment. The



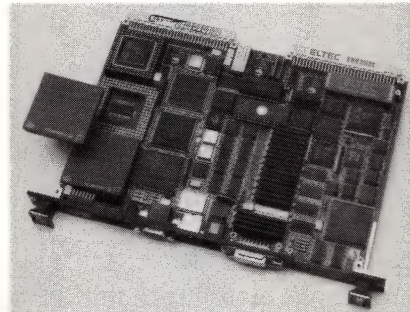
card supports most monochrome and color flat-panel displays, including 8- and 16-bit single- and dual-scan color STN panels, and 9-, 12-, 15-, and 18-bit color TFT panels. It contains 1 Mbyte of video memory and supports CRT resolutions up to 1024 by 768 pixels with 256 colors, noninterlaced. The

ZT 8982 also supplies a PC/AT-compatible keyboard controller. Available now, the interface board sells for \$595. Large-quantity discounts are available. RN

Ziatech Corp., 1050 Southwood Dr., San Luis Obispo, CA 93401;
(805) 541-0488. **CIRCLE 689**

VME CPU BOARD HOLDS DUAL 68040S

Performance specifications of 70 MIPS and 11.9 MFLOPS can be reached by the Eurocomm 17 VME CPU board, which is built with two 40-MHz MC68040 microprocessors. The board features up to 32 Mbytes of DRAM, a VME64 interface, SCSI-2, and an Ethernet port. The high-performance graphics subsystem



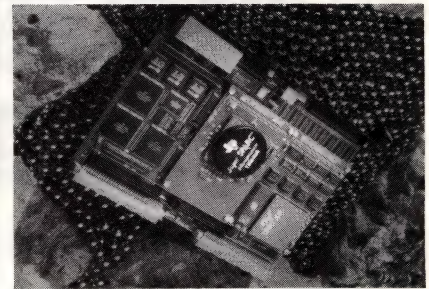
displays 1152 by 900 pixels, while a local-bus mezzanine connector lets users plug in their own customized modules. The two CPUs are coupled to a processor bus, which is also attached to the SCSI controller, the DRAM, and the video RAM. A proprietary I/O controller containing a FIFO buffer avoids interrupting the CPUs during block transfers through the VMEbus. Most popular real-time operating systems are supported. Prices for the Eurocomm 17 start at \$1800. RN

American Eltec Inc., 4340 Steven's Creek Blvd., Suite 204, San Jose, CA 95129; (408) 244-4700.

CIRCLE 690

VME SBC HOLDS MULTIPLE SPARC CPUS

Designed to the Eurocard VME form factor, the V64-SS single-board computer incorporates multiple Super Sparc processors, all capable of running the Solaris and VxWorks operating systems concurrently and independently. The baseboard is split into two separate fully isolated processor-board sections—an accelera-



tor section that handles data at 200 Mbytes/s, and a main processing section. By separating the processing and preprocessing units, the microprocessors can run at their maximum speed.

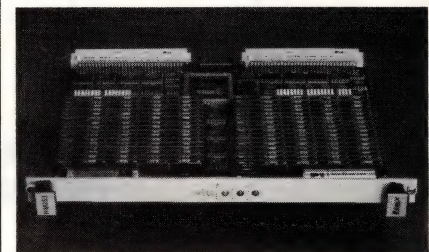
By configuring the board with two SuperSparc CPUs and one i860XP processor, it can handle 240 MIPS and 140 MFLOPS. Even more processing power can be added through the SBus mezzanine bus. Up to 128 Mbytes of DRAM fit on the board. Available now, the V64-SS single-board computer is priced at \$7590. Large-quantity discounts apply. RN

General Micro Systems Inc., 8358 Maple Pl., Rancho Cucamonga, CA 91730; (714) 980-4VME.

CIRCLE 691

VME MEMORY BOARD HOLDS 128 MBYTES

Supporting up to 128 Mbytes of static RAM or flash memory, the RM250 single-slot memory board connects to the VME64 or VMEbus. To achieve fault tolerance, the 6U RM250 can be configured for dual



writes using two memory boards. Each board can be enabled or disabled through software. Two lithium batteries are provided for backup power. A second application for the RM250 is as a cache memory. Modes of operation include read, write, and read-write-modify. Available now, prices for the memory board start at \$1333. RN

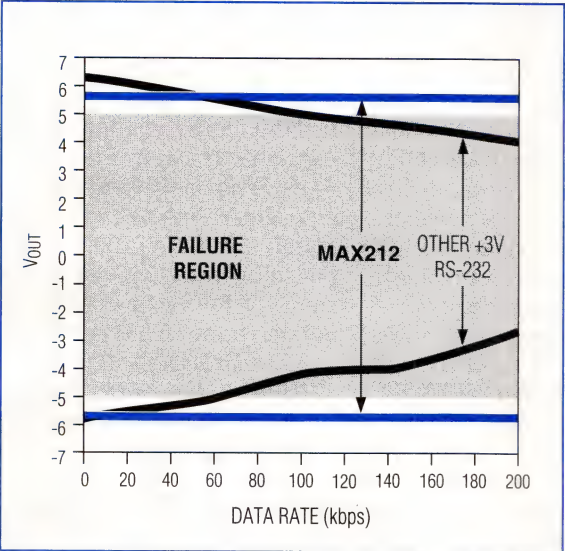
RAMix Inc., 9421 Winnetka Ave., Bldg. K, Chatsworth, CA 91311;
(818) 349-6772. **CIRCLE 692**

TRUE +3V RS-232 IC REDUCES POWER 8 TIMES!

Complete Serial Port Runs at 120kbps & Drives a Mouse @ 3.0V!—GUARANTEED

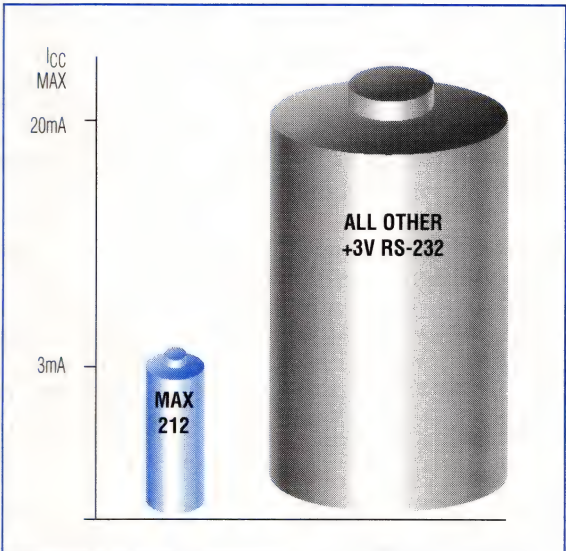
Maxim's new MAX212 has the highest data rate and the lowest power of any 3V RS-232 IC. And, the MAX212 is the only +3V RS-232 transceiver powerful enough to drive a mouse at 3.0V!

120kbps DATA RATE—GUARANTEED!



A regulated output stage guarantees RS-232 output levels are met; even at 120kbps!

REDUCE POWER 8 TIMES!



The MAX212's proprietary architecture reduces power 8 times!

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MAX560	8mA	120	2	Meets Low Power EIA/TIA-562
MAX561	8mA	120	0	Pin Compatible with MAX241



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CONNECT PCI BUS DIRECTLY TO PCMCIA AT 3.3 OR 5 V

Using the CL-PD6729, the PCI bus can be connected directly to the PCMCIA bus, regardless of whether the system runs at 3.3 or 5 V. The dual-slot host-adaptor chip contains a direct connection to the PCI bus. It supports a standard bus interface for systems based on the 80X86, PowerPC, and other standard microprocessors. As a result, the two fully buffered PCMCIA slots can reside on both desktop and portable systems.

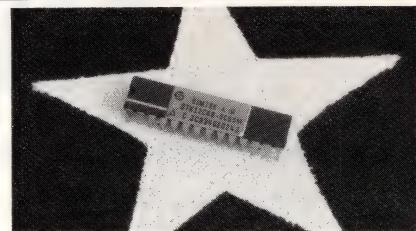
The device complies with the PCMCIA two-pin detection standard for low-voltage cards. In addition, the chip includes a control feature that prevents any damage from occurring to a card in a mixed-voltage environment. Also, the chip's regis-

ter-set compatibility allows existing socket services to operate with the device. Because a complete PCI-bus system can be built, there's no need for an ISA bridge to implement the PCMCIA.

Only 2 in.² are required to implement a dual-slot control subsystem. Universal card support comes from the BIOS-level software that supplies the interfaces between the host-adaptor hardware and the host operating system. The CL-PD6729 PCI-to-PCMCIA IC is housed in a 208-pin quad flat pack. Samples are available now, with production starting sometime this quarter. In quantities of 1000, the chip sells for \$24.

Cirrus Logic Inc., 3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300. CIRCLE 693

■ RICHARD NASS



of 10,000 or 100,000 store cycles; both grades include a ten-year data-retention guarantee. Data is automatically reloaded into the SRAM when power is restored, or when a software Recall command is issued. The STK12C68-M comes in an 8-kword-by-8-bit configuration and has access-time speed grades of 35, 45, or 55 ns. When not run at full speed, the chip draws just 15 mA from a 5-V supply. Initially, the chip will be housed in a 300-mil wide, 28-lead ceramic DIP. In lots of 1000, the 55-ns version costs \$92.33 each. DB

Simtek Corp., 1465 Kelly Johnson Blvd., Colorado Springs, CO 80920; David Bowers, (719) 531-9444. CIRCLE 695

REVAMPED MCUS TRIM SUPPLY LEVELS TO 1.8 V

Aimed at low-power portable applications, seven 68HC05 microcontrollers can operate with power supplies as low as 1.8 V. When powered at 1.8 V, the controllers draw just 300 μ A, when operating at a top frequency of 500 kHz—about one-third the power of equivalent 3-V versions. The low-power versions have an "L" designation: 68HCL05C4, L05C8, L05C12, L05J1A, L05K0, L05P1, and L05P4. The J1A version is used in the cordless MouseMan—a wireless mouse developed by Logitech. The C4 and P4 versions include 4 kbytes of ROM and 176 bytes of RAM, but differ in I/O—the C4 has 24 I/O lines, 7 input-only lines and comes in 40, 42 or 44-lead packages, while the P4 comes in 28-lead DIP or SOIC packages. The C8 and C12 are similar to the C4 but pack 8- and 12-kbytes of ROM. The J1A and K0 carry the smallest memory—1024 bytes of ROM and 64 bytes of RAM, and 512 bytes of ROM and 32 bytes of RAM, respectively. The J1A comes in 20-lead DIPs or SOIC packages; the K0 uses 16-lead versions of the same packages. The P1 comes with 2 kwords of ROM, 128 bytes of RAM,

20 I/O lines, and comes in a 28-lead DIP or SOIC package. The 1.8-V chips start at as little as \$1.07 each. DB

Motorola Inc., 6501 William Cannon Road West, Austin, TX 78735-8598; Julie Kleinkopf, (512) 891-2035. CIRCLE 694

NONVOLATILE SRAM PACKS 64 KBITS

Offering MIL-STD-883 class B compliance, the STK12C68-M nonvolatile SRAM provides 64-kbits of storage backed up by a nonvolatile shadow memory. The chip includes AutoStore, a feature Simtek developed that's now available on its commercial-grade chips. The AutoStore mode continuously monitors the chip's power supply and internal state, and allows the nvSRAM to automatically store all the contents of the SRAM cells into the nonvolatile shadow array, when the chip's pins sense a power loss. When it detects a loss, the AutoStore circuitry disconnects the chip from the main power source and draws power from a small external capacitor (100 μ F), so it can save the SRAM data in the shadow EEPROM array. Versions are available with endurance ratings

BIPOLAR 22V10 TRIMS I/O DELAY TO JUST 5 NS

Able to deliver a top operating speed of 117 MHz, a bipolar 22V10 PLD achieves its high speed thanks to an input-to-output propagation delay of just 5 ns. As with standard 22V10 PLDs, the high-speed chip provides up to 22 inputs, up to 10 outputs, and has variable product-term distribution to allow more complex functions to be implemented. The TIBPAL22V10-5CFN gets its speed from the Impact-XL process that employs low-power Schottky technology and proven titanium-tungsten fuses, and from a low-noise package that has very low inductance and can tolerate higher board noise than some other packages. The package uses JEDEC-approved revolution power-and-ground pinout with center V_{CC} pins. To minimize output skew, the outputs surround the V_{CC} pins. When operating from a 5-V supply, the chip draws a maximum of 210 mA. In lots of 100, the TIBPAL22V10-5CFN sells for \$25.75 when housed in a 28-lead PLCC. DB

Texas Instruments Inc., Semiconductor Group, SC-94003, P.O. Box 655303, Dallas, TX 75265; (214) 997-5666. CIRCLE 696

NEW PRODUCTS

DIGITAL ICs

FREQUENCY MULTIPLIER UPS CLOCKS TO 120 MHZ

As one way to lower the cost of high-frequency oscillators, the ST49C101 is a mask-programmable CMOS circuit that can multiply the output frequency of a low-frequency crystal oscillator to provide high-frequency clocks in workstations, graphics subsystems, and many other applications. Housed in 8-lead mini DIPs or SOIC packages, the preprogrammed versions of the analog frequency multiplier, the ST49C101P8 or ST49C101CF8, accept a 10-MHz reference input and deliver a 120-MHz output clock. Designed for low-power operation, the multiplier chips run from a 5-V supply but operate at power levels below that of digitally based frequency multipliers. The stability of the output frequency is determined by the stability of the input frequency and the divider ratio. Customized multiplication factors can be mask programmed into the analog chip with a turnaround of just

three weeks for production quantities. The DIP or SOIC-housed versions sell for \$3 each in lots of 1000 units. Samples are available now and production quantities currently require about four weeks from receipt of order. DB

Startech Semiconductor Inc., 219 Bordeaux Dr., Sunnyvale, CA 94089; Ram Reddy, (408) 745-0801. CIRCLE 697

FEATURE-RICH 8-BIT MCUS OPERATE FROM JUST 3 V

Enhancing the options for its 68HC11 family of 8-bit microcontrollers, Motorola has created low-voltage versions of 25 different family members. The MCUs that contain on-chip EEPROM and a-d converters are included as part of the family, which can operate at clock frequencies of up to 3 MHz with supply levels of as little as 3-V, or as high as 5.5 V. The most recent additions include the 68HC11F1, the KA0, KA1, KA3, and the KA4. The F1 includes no

ROM or EPROM, but packs 1 kbyte of RAM, and 512 bytes of EEPROM along with 30 I/O lines, and an 8-bit a-d converter. One of the other chips, the KA4, comes with 24-kbytes of ROM or EPROM, 768 bytes of RAM, 640 bytes of EEPROM, over 50 I/O lines, and an 8-bit a-d converter. Several EPROM-based versions, some containing EEPROM, were also released with 3-V supply operation—the 68HC711D3, E9, and L6. The D3 includes 4 kbytes of EPROM, 192 bytes of RAM, 32 I/O lines, and operates at speeds of up to 2 MHz, while the E9 comes with 12 kbytes of EPROM, 512 bytes of RAM, 512 bytes of EEPROM, an 8-bit a-d converter and 38 I/O lines. The L6 adds another 4 kbytes of EPROM and more I/O lines. Prices for the 3-V chips are \$4.34 to \$21.28 each in lots of 10,000. DB

Motorola Inc., Microcontroller Div., 6501 William Cannon Dr. W., Austin, TX 78735-8598; Judy Racino, (512) 891-3465. CIRCLE 698

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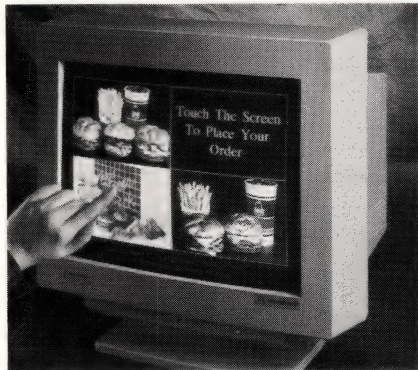


NEW PRODUCTS

COMPUTERS & PERIPHERALS

17-IN. DISPLAY ADDS TOUCH FUNCTIONALITY

The TruePoint-DS17 Touch Monitor is a 17-in. flat, square display that adds touch-screen capabilities. It in-



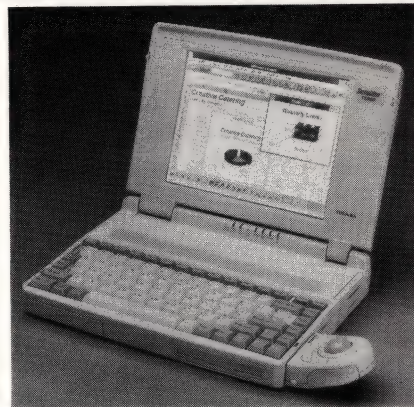
tegrates a high-resolution Mitsubishi Diamond Scan 17FS CRT with an analog capacitive touch screen and controller, and all the necessary software drivers. The touch functions come from a transparent thin-film conductive coating that's fused to the display's glass surface. A glass overcoat protects and seals the sen-

sor. The monitor supplies high-refresh, flicker-free resolutions up to 1280 by 1024 pixels at 74 Hz noninterlaced. It also incorporates a dot pitch of 0.28 mm, a vertical scan range of 50 to 130 Hz, and a horizontal scan rate of 30 to 78 kHz. Available now, the TruePoint-DS17 sells for \$1975. Large-quantity discounts are available. RN

MicroTouch Systems Inc., 300 Griffin Park, Methuen, MA 01844; (508) 659-9100. CIRCLE 699

NOTEBOOK HOLDS SL ENHANCED 486SX

A 33-MHz SL Enhanced 3.3-V 486SX microprocessor forms the brains of the T1910 notebook computer. The 6.5-lb. system comes with a choice of a color or monochrome 9.5-in. flat-panel display. System memory ranges from 4 to 20 Mbytes, while the hard-drive options run from 120 to 200 Mbytes. The computer's 14.5-mm "hot-pluggable" PCMCIA slot can handle cards of any standard

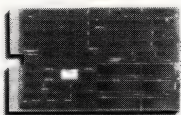
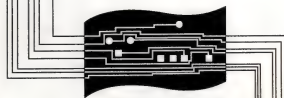
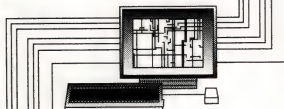
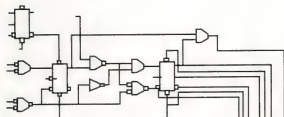


form factor. The built-in NiMH battery supplies better than 3 hrs. of computing life and a 2.3-hr. recharge time. Preinstalled software includes MS-DOS 6.2, Windows 3.1, and Ultra-Font (a drawing package). A trackball is included. Prices range from \$1599 to \$2499, depending on the bundled options. RN

Toshiba America Information Systems Inc., P.O. Box 19724, Irvine, CA 92713; (800) 334-3445. CIRCLE 700

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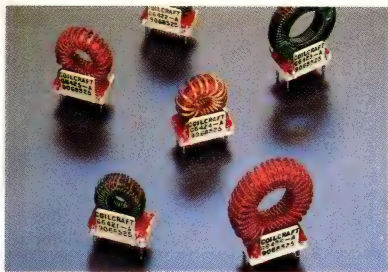
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High performance mag amps feature amorphous cores

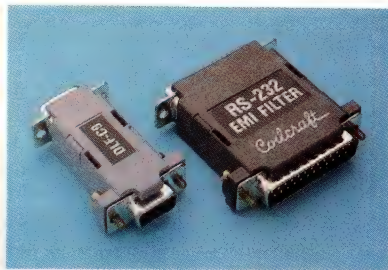
Coilcraft offers a series of high performance saturable reactor (mag amp) inductors for regulating switching power supplies. They're ideal for outputs over 2 Amps and cross regulation in multi-output supplies.

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By using amorphous alloy core materials, these mag amps offer extremely low loss, especially at high frequencies (100 kHz and up). They require lower reset current compared to parts with nickel-iron alloy cores, as well as high BSAT.

For more information contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

READER SERVICE 150



EMI filters reduce noise in RS-232 signal lines

Coilcraft's new EMI Filter Modules are an easy, effective way for users to eliminate the problems of stray electromagnetic interference (EMI) in signal cables running between poorly filtered equipment.

Available in DB-25 and DB-9 versions, the modules plug between an RS-232 cable and an input or output port. Common mode magnetics filter all lines including the frame ground, attenuating EMI as much as 19 dB over the critical 30 - 300 MHz range while leaving data signals totally undisturbed.

Comparable EMI filters for circuit board mounting are also available.

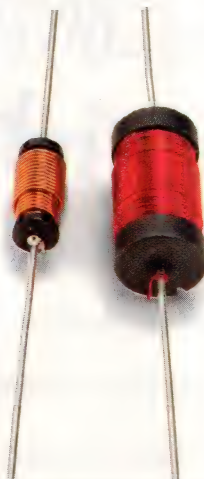
For more information contact **Coilcraft**, 1102 Silver Lake Road, Cary IL 60013. 708/639-6400.

READER SERVICE 149

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Our .45" diameter PCH-45 Series is rated for 14.3 Amps DC at 3.9 μ H. Other parts provide up to 100 mH inductance.

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Order our low-cost Designer's Kit with 60 standard values to use in your prototypes. Or call us and we'll custom-engineer a choke to fit your needs.

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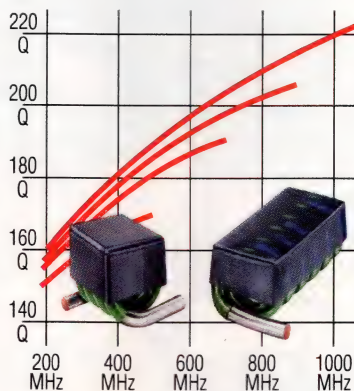
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READER SERVICE 148

Now you can get the high Q of an air core inductor. Plus the convenience and cost savings of a true surface mount component.

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READER SERVICE 147

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FIRST POWERPC MACS DELIVER MANY FEATURES

Three desktop computers based on the PowerPC 601 RISC processor represents Apple Computer's first Macintosh-compatible RISC-based systems. The three machines, in order of performance, include the 6100/60, 7100/66, and the 8100/80, which are based on 60-, 66-, and 80-MHz versions of the PowerPC 601. For native-mode applications, the 6100/60 delivers between two- to four-times the performance of a 68040 running at 33 MHz; for emulated 680x0-based software, the same platform delivers performance equivalent to a fast 68030 to 68040 system. The 7100/66 system runs about 25% faster than the 6100/60. The top-of-the-line 8100/80 delivers about twice the throughput of the first system.

Neither the 60- nor the 66-MHz systems include any secondary cache, but the 80-MHz unit has a 256-kbyte cache as standard. All three systems come with 8 Mbytes of RAM, and both an asynchronous SCSI port and a DMA-supported Ethernet port are included. All models also come with a video-input capability that supports NTSC, PAL, and SECAM, and handles video in a resizable window. Video output in NTSC or PAL formats, as well as an S-video I/O port, also comes on all models. The video I/O goes through a new connector interface on the rear panel of all the systems. LocalTalk and GeoPort-compatible serial interfaces are included, as is a 16-bit stereo audio I/O port and an Apple Desktop Bus port for input devices.

NuBus expansion slots are included in all systems—one 7-in. card in the 6100/60 and three full-size cards in the other two models. Memory expansion beyond the base memory goes from 72 Mbytes (in the 6100/60) to 136 Mbytes (in the 7100/66), and peaks at 264 Mbytes (in the 8100/80). All systems come with a DMA-supported floppy drive, and with 160 to 250 Mbytes of hard-disk storage in the base models. The high-end system holds disk drives capable of up to 1 Gbyte. A CD-ROM drive is optional

on all systems. The 8100/80 also comes with a second SCSI channel, so slow peripherals won't bog down higher-speed ones.

Video frame buffer support starts with DRAM-based video memory on all models, but the 7100/66 and 8100/80 include higher-performance VRAM-based frame buffers of 1 Mbyte and 2 Mbytes, respectively. One 14- or 16-in. display monitor is supported by the 6100/60 (16-bit color on the 14-in., and 8-bit color on the 16-in. monitor), while with the VRAM-based video adapter, the 7100/66 and 8100/60 support up to 21-in. monitors with up to 24-bit color. The systems will all run the Macintosh System 7.1.2 operating system and come with AppleScript, PC Exchange, and QuickTime software. The system also has PlainTalk, a text-to-speech and speech-recogni-

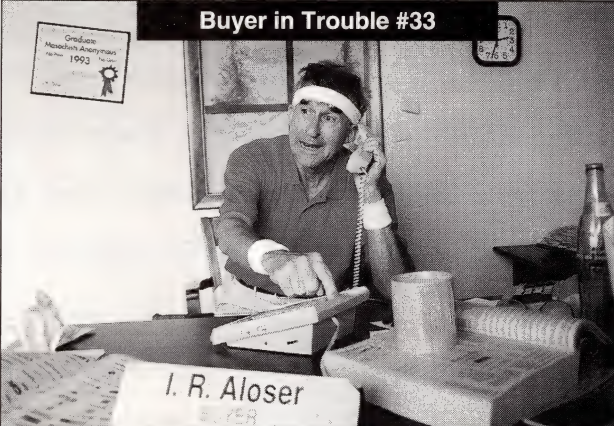
tion software package, and MS-DOS/Windows emulation through the Insignia Software SoftWindows emulator.

The 6100/60 comes in a low-profile pizza-box enclosure, the 7100/66 comes in a moderate-height desktop cabinet, and the 8100/80 comes in a mini-tower-style cabinet. Initial prices are \$2000, \$3000, and \$4000, respectively, for the 60-, 66-, and 80-MHz systems. An upgrade card for 68040-based Macintoshes is also available for the processor-direct slot. Prices for the PowerPC Macintoshes are \$1819, \$2899, and \$4249, respectively, for just the 60-, 66-, and 80-MHz CPU box, and increase to \$2209, \$3379, and \$4869, respectively, for systems with a color monitor and keyboard. The Power Macintosh upgrade card sells for \$699.

Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014; Brodie Keast, (408) 996-1010. **CIRCLE 101**

■ DAVE BURSKY

Buyer in Trouble #33



"You're Gonna Deliver When?!!"

When is St. Patrick's Day? I promised Rocky in production they would be here last week!
(CLICK!) Hello...Hello...

I shoulda called Prem for pc power transformers. I hear they deliver when you need them,

I really shoulda called Prem.

You oughta call Prem!"



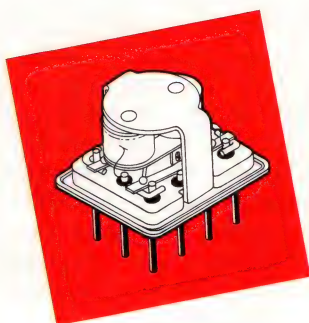
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READER SERVICE 127

THE HIGH PERFORMANCE GIGAHERTZ RELAY



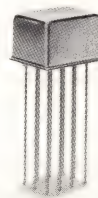
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- Magnetic latching cuts power drain
- Convenient Centigrad® package
- Aerospace and commercial versions

The TO-5 family of relays are great performers in RF switching applications. They are inherently that way. Low inter-contact capacitance. Low insertion loss. Up through 500 MHz. No problem.

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The high performance gigahertz Centrigrid® relay (RF 170) will handle your toughest switching assignments, especially when power drain is critical. For price, delivery, and more technical information, call **1-800-284-7007** or Fax us at 1-213-779-9161.



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NEW PRODUCTS

SOFTWARE

DESIGN CONTROLLERS FOR NONLINEAR SYSTEMS

The Nonlinear Control Design Toolbox, said to be the first commercial product for designing automatic controllers for nonlinear systems, is intended for engineers who design controllers applied in automotive, aerospace, and process control. The toolbox enables engineers to design controllers directly in the nonlinear domain, bypassing linear-approximation and other ad hoc steps previously required. The toolbox extends the company's Simulink block diagram environment for modeling analyzing dynamic systems. The user places one or more NCD blocks in a system model and then graphically describes constraints on the system time response with the mouse. The toolbox can be used to tune multiple controllers within a system. The designer can use MonteCarlo simulations to design controllers even when there are uncertainties or variations in the system's components. Pricing begins at \$895 for the Windows version. SVT

The MathWorks Inc., 24 Prime Park Way, Natick, MA 01760; (508)653-1415; fax-2997. CIRCLE 702

PROGRAM TAKES A SOFTWARE INVENTORY

NetCensus version 2.0 software automatically tracks hardware and software components on networked and standalone workstations. With the software, users can monitor changes, find underused PC components, plan and budget for upgrades and growth, and control use of non-standard and unauthorized software. NetCensus identifies software by brand name, version number, embedded serial number, and foreign language edition. Version 2.0 requires a 386-based, IBM-compatible PC as an administrator with 5 Mbytes of hard disk space, 4 Mbytes of RAM, DOS 3.3 or later, and Windows 3.1. Prices range between \$10 and \$20 per PC, depending on the total number of PCs. Product upgrades are free for a year with orders of 50 or more licenses. SVT

Tally Systems Corp., P. O. 70, Hanover, NH 03755; (800) 262-3877 or (603) 643-1300; fax - 9366. CIRCLE 703

WINDOWS-BASED COMM SOFTWARE OPERATES IN THE BACKGROUND

By running Version 1.0 of the QModemPro for Windows communications program, users can upload or download files in the background, while running other applications in the foreground. In addition, the software supports both data and fax transmissions. Faxes can be sent or received using any Class 1 or 2 fax modem. A host of transfer protocols are supported, including ASCII, Compuserve B+, Kermit, and variations of XModem, YModem, and ZModem. In addition, QModemPro for Windows supports almost all standard terminal emulations.

Another feature built into the package is the ability to upload files using a drag-and-drop procedure, going from the Windows File Manager to QModemPro's upload window.

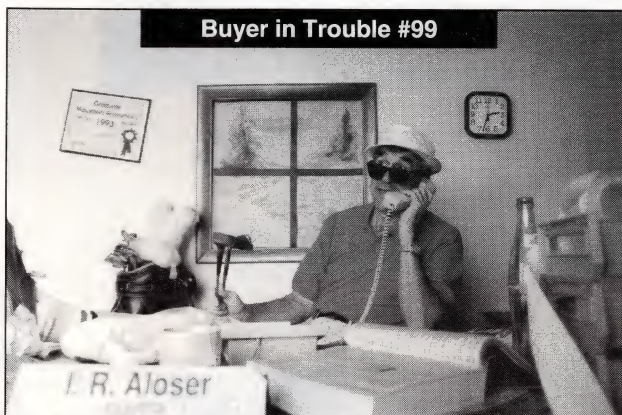
Portions of files can be marked and copied to the Windows clipboard. Sound cards are supported, enabling different sounds to be attached to such functions as connect, dialing, failures, and file-transfer success. Another feature of the software is the ability to view .GIF files while downloading.

Full support is included for asynchronous connection to PCs, Macs, minicomputers, mainframes, and most popular on-line information suppliers. Available now, QModemPro for Windows sells for \$139. Users of earlier versions of QModem communication software can upgrade for \$50.

Mustang Software Inc., 6200 Lake Ming Rd., Bakersfield, CA 93306; (800) 999-9619 or (805) 873-2500. CIRCLE 704

■ RICHARD NASS

Buyer in Trouble #99



Losing the Golf War

"Rocky. This new catalog's not only got transformers, it's got golf balls guaranteed to go 400 yards. Don't scream, Rocky. I didn't know Prem had a new catalog.

But think about it, Rocky, 400 yards...

(CLICK!) Rocky?? Hello...Hello...

I really shoulda called Prem.

You oughta call Prem!"



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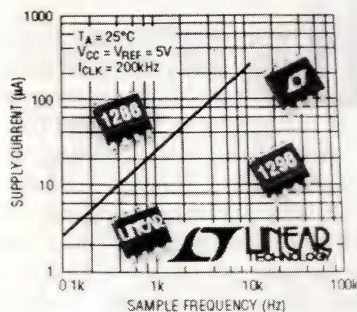
READER SERVICE 128

MICROPOWER 12-BIT A-D CONVERTER PAIR NEEDS JUST 20 μA I_q SAMPLING AT 1 KHz

The demand for integrated circuits needing ever-lower operating power, supply voltage, and size continues to have an impact upon the instrumentation arena as well as that of the personal computer.

Meeting these needs are a pair of micropower 12-bit sampling analog-to-digital converters in 8-pin dual in-line packages and small outline integrated circuits.

While these siblings are designed to run off 5-V to 9-V rails, 2.7-V versions are just around the corner. Called the LTC1286 and LTC1298, only the analog inputs of the analog-to-digital converters differ. The former ADC sports one differential input; the latter offers a software selectable two-channel multiplexer. On-chip serial ports provide efficient



data transfer, over three wires, to a wide range of microprocessors.

The two converters' quiescent current, a direct function of the sampling rate, ranges from less than 5 μA , while sampling at 100 Hz, to 250 μA , when sampling at the maximum rate of 12.5 kHz. Moreover, when not converting, the a-d converters automatically shut down and draw less than 3 μA .

The a-d converters' switched-capacitor SAR architecture provides inherent sampling. The supply rail can be used as a reference, or an external reference can be used.

Typical ac specifications are provided for 1-kHz inputs, while sampling at 12.5 kHz. For those conditions $S/(N+D) = 72$ dB, $\text{THD} = -80$ dB, and $\text{SFDR} = 80$ dB. At dc maximum integral linearity error = ± 2 LSB, however, "no-missing-code operation" is guaranteed to 12-bits. Maximum gain and offset error run ± 8 and ± 3 LSB, respectively.

In quantities of 1000, the DIP costs \$4.65 and \$5.00 each, respectively.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 4-LINEAR.

CIRCLE 705

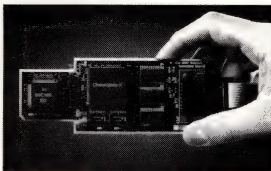
FRANK GOODENOUGH

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READER SERVICE 86

152 E L E C T R O N I C D E S I G N

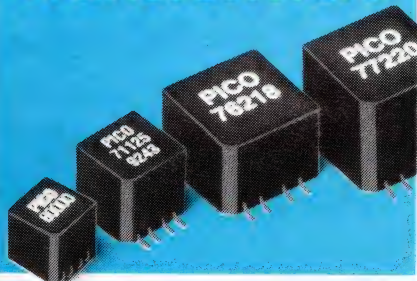
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PICO surface mount units utilize materials and methods to withstand extreme temperature (220°C) of vapor phase, I.R., and other reflow procedures without degradation of electrical or mechanical characteristics.

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READER SERVICE 161

NEW PRODUCTS

COMMUNICATIONS

DUAL-CHANNEL LAN/WAN ANALYZER OFFERS LOW-COST, HIGH PERFORMANCE

Using a powerful embedded processor and modular I/O modules, the RC-100WL analyzer permits network managers to perform simultaneous monitoring or troubleshooting of two LAN or WAN systems. The high processing rate of the unit's Intel 960 embedded processor gives it a throughput of up to 2 Mbps for WANs, and a 16 Mbps for LANS. The dual-channel system can perform internetwork analysis tasks, such as simultaneously testing both sides of a bridge or router.

Weighing 4 lbs., the analyzer is compact with the form factor of a slim notebook computer. Instead of incorporating the bulk of a dedicated display and keyboard into the analyzer, the RC-100WL is controlled via the parallel port of any Windows-based computer. Consequently, users can use an existing PC as a non-dedicated controller or buy a dedicated, low-cost desktop or laptop. The modular I/O section of the RC-100WL allows each channel to support a different physical interface. Available now are modules to support V.35, T1, FT1, E1, RS449/530/232, X.21, Ethernet, and Token Ring. With optional software packages, each system channel can be config-

ured to support monitoring and simulation of many standard protocols, including Frame relay, SMDS, X.25, Async, TCP/IP, IPX, and DECnet. When used in dual-channel mode, the analyzer can be inserted between any combination of LANs and WANs. This allows the operator to obtain a real-time picture of the traffic on each network, as well as the flow of data between them.

The graphical-interface-based software provided for the analyzer provides network managers with a powerful suite of analysis tools. Used in a conventional manner, the instrument can employ one channel to either perform analysis on existing network traffic, or insert its own simulated data. The encapsulation analysis software provided with the RC-100WL lets it extract and analyze data even when it's embedded in several layers of protocol—for example, a TCP packet carried as IP data within frame relay. By employing a standard PC for the user interface, and using large-scale integration, production costs were kept low. The base unit is \$9000.

RadCom Corp., 900 Corporate Dr., Mahwah, NJ 07430; Avi Zamir, (210) 529-1100. **CIRCLE 706**
■ LEE GOLDBERG

CHIPSET FOR GSM II CELLULAR PHONES

A three-chip set comes with all of the baseband functions for GSM-2 cellular handsets. GSM phase 2 is the enhanced version of the European cellular telephone standard. Requiring only a radio subsystem and memory, the AD20msp410 chip set includes a phase-2 software suite, which provides support for GSM's enhanced features, such as direct transmission of digital information. The set consists of the physical layer processor (PLP), an algorithm signal processor (ASP), and a dedicated mixed-signal processing device called the baseband converter (BBC).

The PLP performs all channel-coding functions, and implements all ap-

plication software and GSM protocols via an embedded 16-bit microcontroller. The ASP performs all speech coding and soft decision equalization. The BBC includes CODECs and implements all mixed-signal radio, audio, and auxiliary functions of the terminal. The chip set operates on a 3- or 5-V supply and features several power-saving modes, which can provide over two hours of talk time and a standby time of over 40 hours. All components, including an evaluation board are sampling now. The chip sets and software will come separately or together for less than \$50 in OEM quantities.

Analog Devices Inc., 181 Ballardvale St., Wilmington, MA 01887; (617) 937-1428. **CIRCLE 707**

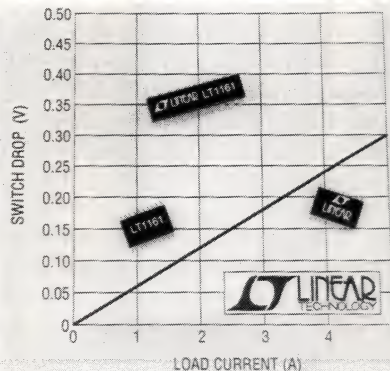
NEW PRODUCTS

POWER

DRIVER TURNS ON 4 HIGH-SIDE FETs WHILE LIMITING THEIR CURRENT

Designed to provide high-side drive for a quartet of n-channel power MOSFETs, the LT1161 quad driver also protects the FETs by providing user-programmable current limiting. With the use of four internal charge pumps, this power-control IC shifts 5-V CMOS/TTL logic levels to 8 to 12 V above the supply rail required to fully enhance typical n-channel power MOSFETs in high-side dc-switching applications. Bringing each of the logic inputs high turns on a separate charge pump, which in turn brings one of the four outputs high. The circuit brings the output at least 4 V above an 8-V rail, 7 V above a 12-V rail, and at least 10 V above any supply rail between 24 and 48 V, the maximum operating voltage.

Each switch channel also includes a drain-sense comparator, which monitors the voltage across a low-resistance, user-selected resistor inserted between the drain of the FET and the supply rail. When the drop across the resistor exceeds 62 mV, the chip turns off the FET's drive and starts an RC timer. The drive is



kept off for a period of time set by the timer's external capacitor. When timed out, it automatically tries to restart (turn on) the FET. If the fault causing the high current still exists, the cycle repeats itself until the fault is removed, protecting the FET and its load.

The LT1161 comes in both commercial and industrial temperature grades and in both 20-pin DIPs and SOICs. The plastic DIP goes for \$3.44 each in lots of 1000.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 4-LINEAR.

CIRCLE 708

■ FRANK GOODENOUGH

9-TO-3-V CONVERTER SUCKS LAST ERG FROM 9-V TRANSISTOR BATTERY

Major tasks for battery-powered systems include squeezing the last mill coulomb of energy from the battery itself—over the widest range of load current. Efficiency is key when the energy source is a tiny 9-V battery. Meeting this requirement is a trio of buck converters, the MAX639, MAX640, and the MAX653, with fixed outputs of 5 V, 3.3 V, and 3 V, respectively. Each includes a controller and a large, on-chip pMOS power switch. Input-voltage ranges for all three run from 4 V to 11.5 V.

While operating from a 9-V battery, the efficiency of the MAX639 typically runs 91% when handling a 100-mA load, and 94% when handling 25 mA. At similar loads, the MAX640

runs 87% and 91% efficient, respectively, and the MAX653 runs 85% and 89% efficient. With a low quiescent current of 20 μ A maximum, the typical efficiency at load currents as low as 1 mA runs from 85% to 95%. Running off a 9-V battery, the on-resistance of the on-chip switch is 1.5 Ω maximum for all three devices. Connected to a 4-V supply rail, the on-resistance of the MAX640 and MAX653 is 2.8 Ω maximum.

All three dc-to-dc converters come in 8-pin DIPs and SOICs. In quantities of 1000, pricing starts at \$2.15 each.

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600, ext. 6087. CIRCLE 709

■ FRANK GOODENOUGH

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Low Noise OXCOs (4 - 25MHz)

MODEL	CO-717L2	CO-718SL2
Aging	1 x 10 ⁻⁹ /day 3 x 10 ⁻⁷ /yr	5 x 10 ⁻¹⁰ /day 1 x 10 ⁻⁷ /yr 2-5 x 10 ⁻⁸ /yr o
0°C to 50°C -20°C to +70°C	±1 x 10 ⁻⁸ ±3 x 10 ⁻⁸	±5 x 10 ⁻⁹ ±1 x 10 ⁻⁸
Phase 100Hz Noise 1kHz (4-12MHz) 50kHz	-145dBc/Hz -160dBc/Hz -165dBc/Hz	-155dBc/Hz -163dBc/Hz -168dBc/Hz
Size	2"x2"x1"	2"x2"x1"
*3/4" height optional		

Low Noise OCXOs (25 - 200MHz)

TYPE	CO-724SL2	CO-725SL2
Aging	2 x 10 ⁻⁹ /day 5 x 10 ⁻⁷ /yr	5 x 10 ⁻¹⁰ /day 1 x 10 ⁻⁷ /yr
0°C to 50°C -20°C to +70°C	±5 x 10 ⁻⁹ ±1 x 10 ⁻⁸	±5 x 10 ⁻⁹ ±1 x 10 ⁻⁸
Phase 100Hz Noise 1kHz (75-125 MHz) 50kHz	-130dBc/Hz -145dBc/Hz -157dBc/Hz	-120dBc/Hz -135dBc/Hz -140dBc/Hz
Size	2"x2"x1"	2"x2"x1 1/4"
*Reduced height available		

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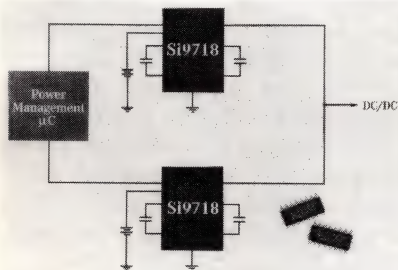
READER SERVICE 140

NEW PRODUCTS

POWER

REVERSE-BLOCK SWITCH SIMPLIFIES PC DESIGNS

A reverse blocking switch for battery-disconnect applications simplifies the design of power-supply circuitry for portable computers. Replacing two MOSFETs and associated drive circuitry, the Si9718CY switch eliminates a problem that's common to many dual-battery-pack devices by allowing the computer to switch from one pack to the other be-

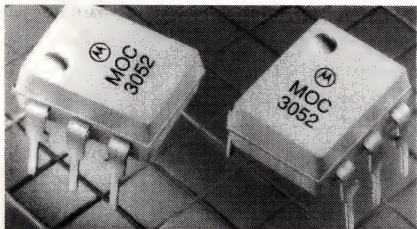


fore battery cells are completely discharged. The device is also useful in designs with auxiliary power sources, such as automotive cigarette lighters. Built on a lateral process, the reverse blocking component of the Si9718CY eliminates the parasitic diode typical in standard MOSFET technologies. Rated at 80 mΩ and 3.5 A, the device also includes charge-pump and Enable circuitry. Pricing is \$2.95 in 100,000-piece lots. Samples are available now with production lead times running 8 to 10 weeks. DM

Siliconix, 2201 Laurelwood Rd., P.O. Box 54951, Santa Clara, CA 95056-0951; (800) 554-5565, ext. 18. CIRCLE 710

OPTO TRIAC DRIVERS ISOLATE LOGIC FROM LINE

A series of 600-V, random-phase opto triac drivers consists of a GaAs in-



frared LED optically coupled to a non-zero-crossing, silicon bilateral ac switch (triac). The MOC3050 Series of devices is designed to isolate low-voltage logic from 120- and 240-V ac lines to provide random-phase control of high-current triacs or thy-

ristors. These devices feature greatly enhanced static dv/dt capability to ensure stable switching performance of inductive loads. Applications include solenoid/valve controls, lamp ballasts, interfacing microprocessors to 120- and 240-V ac peripherals, motor controls, and more. Pricing is \$0.70 in lots of 1000. Samples are from stock and lead time for production lots is 6 weeks. DM

Motorola Inc., 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-3879. CIRCLE 711

MODULAR CONVERTERS MAKE SAFETY GRADES

The XWR Series of modular 3-, 10-, and 20-W switching dc-dc converters are now UL-recognized (UL 1950), CSA-certified (C22.2, No. 234), and component IEC 950 registered. Available in single-, dual-, and triple-output versions, the high-efficiency modules are also offered in three wide dc-input-voltage ranges of 4.7 to 7 V, 9 to 18 V, and 18 to 72 V. Output choices include 5, 12, 15, ± 5 , ± 12 , ± 15 , 5/ ± 12 , and 5/ ± 15 V. Delivery is from stock to four weeks. Evaluation samples are available to qualified customers. Call for pricing. DM

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; (508) 339-3000. CIRCLE 712

200-W SWITCHERS BOAST AUTO-RANGING

With features including a 90-to-130-/180-to-264-V ac auto-ranging input, the PU200 Series of ac/dc power supplies offer built-in EMI filter that limits conducted emissions to FCC and VDE Level B standards. A power-fail-detect signal is another feature, as is typical efficiency of 70% and a minimum holdup time of 20 ms. Safety features include short-circuit protection with automatic recovery, over-voltage protection on the main output, and safety ground leakage current of 0.8 A at 115 V ac. Single-quantity pricing starts at under \$200 with OEM quantity prices as low as \$90. Delivery is from stock to 4 weeks for sample lots. DM

International Power Sources Inc., 200 Butterfield Dr., Ashland, MA 01721; (508) 881-7434. CIRCLE 713

MICRO-T OSCILLATORS SLASH SPACE

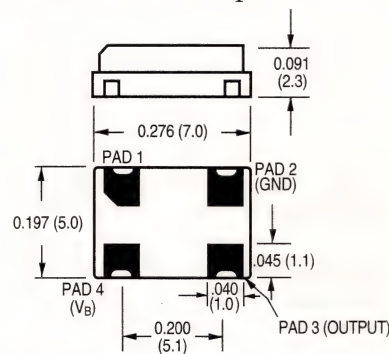
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T1282	Fixed	.005%	0 to 70°C	5V $\pm$ 0.5V
T1258	Fixed	.01%	-40 to +85°C	5V $\pm$ 0.5V
T3290	Tristate	.01%	0 to 70°C	5V $\pm$ 0.5V
T3292	Tristate	.005%	0 to 70°C	5V $\pm$ 0.5V
T3258	Tristate	.01%	-40 to +85°C	5V $\pm$ 0.5V

MF Electronics

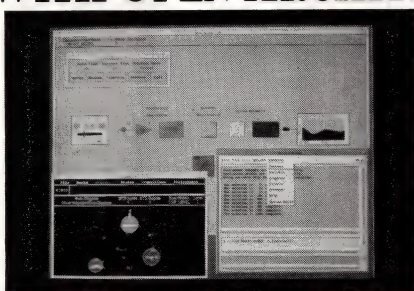
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CONTROL-SYSTEM DESIGN ENVIRONMENT WIDENS APPLICATION RANGE WITH OPEN ARCHITECTURE

An open architecture and new design-documentation tool are just two of the enhancements embedded in the fourth-generation Matrix_x product from Integrated Systems Inc. (ISI). Also new is the adoption of the company's Xmath math software as the system's main analysis environment.

The Matrix_x 4.0 open architecture makes it easy for ISI to add new tools into the environment. It also simplifies the task of integrating existing ISI or third-party analysis, modeling, and simulation modules that bridge the gap between Matrix_x and other CAE environments. These tight links with other tools transform Matrix_x from a specialized control-system design tool into a wide-ranging embedded-system design



environment.

AutoDoc is the new documentation tool that's been added to the Matrix_x system. It uses models and simulation results to automatically generate detailed design documentation of applications created in the Matrix_x environment. AutoDoc outputs can include tables of I/O interfaces, state-transition diagrams, annotated control-block models, and global variables. In addition, AutoDoc out-

puts are compatible with industry-standard Interleaf and FrameMaker electronic-publishing software.

ISI's existing Xmath software is Matrix_x 4.0's standard process- and control-analysis system. Xmath features object-oriented scripting, 2D and 3D graphics, and a programmable graphical user interface. And the Xmath library of special-purpose modules, including those for signal analysis and robust control, now function in the Matrix_x environment.

Initial shipments of Matrix_x 4.0 begin this month for HP and Sun workstations. DEC, IBM, and Silicon Graphics platforms will also be supported. Pricing starts at \$10,000.

Integrated Systems Inc., 3260 Jay St., Santa Clara, CA 95054-3309; (408) 980-1500. CIRCLE 714

■ LISA MALINIAC

VHDL TOOL IMPROVES DESIGN PRODUCTIVITY

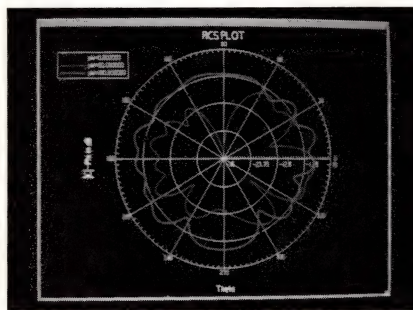
Xpert HDL is a VHDL specification and management tool for both individual engineers and engineering teams. It helps control top-down design of ICs and systems. Engineers use Xpert HDL to establish a consistent VHDL development environment that improves code quality and increases productivity for specification, simulation, and synthesis operating in a top-down methodology. The tool combines a IEEE 1076-compliant VHDL parser with an object-oriented browser and text editor. The browser understands design hierarchy and the relationships between constructs and entities in a VHDL description. Xpert HDL's text editor checks for syntax errors on-line as code is entered, and automatically completes VHDL constructs using keystroke macros. Predefined templates speed design capture for all standard VHDL constructs, and lets users customize to enforce coding styles across large design teams. Users can execute checks to ensure that their VHDL code is synthesizable in either Synopsys or Viewlogic tools. Xpert HDL flags conditions where simulation

and synthesis results will differ due to, for example, problems with signal initialization or sensitivity lists. In addition, on-line help assists both novice and experienced VHDL users. Xpert HDL, available now for Sun workstations, costs \$7500. LM

Summit Design Inc., 9305 S.W. Gemini Dr., Beaverton, OR 97005; (503) 643-9281. CIRCLE 715

MULTI-PLANE SOLVER IS FAST AND ACCURATE

A multi-plane inductance, resistance, and current solver from Contec Microelectronics analyzes planar structures quickly and accurately.



Called ContecPlane, the solver can be used to investigate ground bounce, simultaneous-switching noise and crowding, current distribution, placement and sizing of decou-

pling capacitors, meshed versus solid planes, split planes, power dissipation, and minimum-plane thickness. The product is efficient enough to solve large or finely meshed structures. With ContecPlane, engineers can quickly investigate trade-offs in pc-board and multichip-module designs because once the planar structure has been solved, they can use the same solution in multiple interactive Spice runs. ContecPlane uses efficient techniques to solve for the inductance and resistance of multiple planes and traces in the presence of the planes. It also solves for mutual inductive coupling between planes, and includes the effects of voids that cause nonuniform current distributions. ContecPlane outputs current distribution plots and reduced n-port Spice subcircuit models of the structure. The n-port models can be used for transient, ac, and dc simulations using the company's ContecSpice simulator. ContecPlane is available now for HP and Sun workstations. It can be purchased alone for \$15,000, or can be bundled with the company's other software tools. LM

Contec Microelectronics USA Inc., 2188 Bering Dr., San Jose, CA 95131; (408) 434-6767. CIRCLE 716

ARCHITECTURAL SYNTHESIS CONNECTS TO LOWER-LEVEL DESIGN TOOLS USING BACKPLANE TECHNOLOGY

An architectural-synthesis tool from Viewlogic connects with lower-level logic-synthesis tools through the company's open backplane technology. Called ViewArchitect, the high-level synthesis product elevates the design abstraction at which engineers work. Then, users feed their high-level descriptions directly into the logic-synthesis tool of choice through a synthesis backplane.

ViewArchitect is based on technology from both Viewlogic and Racal-Redac. Users describe, simulate, and synthesize system behavior at a high level of abstraction using VHDL. They can synthesize the architectur-

al design into block diagrams automatically, and analyze trade-offs to arrive at the best architecture prior to implementation.

The tool provides early design verification prior to implementation, and improves users' ability to predict, trace, and control synthesis results. It also helps users meet design-for-testability constraints through the insertion of test structures across an entire chip during the design's architectural phase.

Users have access to a backplane-like capability that lets them feed architectural designs to a variety of logic-synthesis tools for structural implementation. ViewArchitect generates output for all available logic-

synthesis tools, including those from Compass Design Automation and Synopsys.

ViewArchitect costs \$25,000. The initial version will be integrated into the company's Unix-based PowerView design environment. In conjunction with the introduction of ViewArchitect, Viewlogic has slashed the price of its logic-synthesis tool by over 50%. That tool, called ViewSynthesis, now costs \$9000 for Unix platforms and \$7000 for PC-based Windows environments.

Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881. **CIRCLE 117**

■ LISA MALINIAK

NAVIGATOR SIMPLIFIES FPGA DESIGN PROCESS

An intelligent design-management tool from Data I/O simplifies and streamlines the CPLD and FPGA design process. The company has integrated the tool, called Synario Project Navigator, into its Synario Universal FPGA Design System for Windows. Project Navigator combines built-in device knowledge with results-oriented processing to quickly move users from design entry through implementation. The system comes equipped with detailed information regarding the design flow for over 350 FPGA, CPLD, and PLD device architectures. It uses this knowledge to present a checklist of processing steps customized for the target device. Each time users select a new device, Project Navigator reconfigures the design flow and presents a new processing checklist. Throughout the design process, the Navigator implements results-oriented processing. This means that users point-and-click on the desired result, and then Synario performs all the processes needed to obtain that result. Synario pricing starts at \$2995. LM

Data I/O, 10525 Willows Rd. N.E., P.O. Box 97046; Redmond, WA 98073-9746; (800) 332-8246 or (206) 881-6444. **CIRCLE 118**

EDA TOOL CONSIDERS FABRICATION ISSUES

The ATTDFF design-for-fabrication software package is the second product in AT&T Design Automation's design-for-manufacture series. The tool accounts for the fabrication process using design rules, audits, and design-rule checks. Fabrication issues that are covered include drilling, conductor-pattern definition, plating and etching, solder mask, solder-paste and nomenclature-pattern definition, and bare-board test. The broad set of design rules are not hard coded in static component libraries like they are in many existing pc-board CAD systems. Instead, they are set up in interchangeable design-rule libraries that let ATTDFF be used for many manufacturing locations having varying levels of sophistication and manufacturing capability. The tool's Design Profiler generates a report summarizing the key requirements of the design, which allows the factory to formulate an upfront estimate of costs and processes. ATTDFF runs on HP and Sun workstations, and will be available early in the third quarter. A floating license costs \$25,000. LM

AT&T Design Automation, Room 1M-412, 101 Crawfords Corner Rd., Holmdel, NJ 07733; (800) 336-5256. **CIRCLE 119**

GRAPHICALLY CREATE PROGRAMMABLE LOGIC

Warp3 is a graphical software environment from Cypress Semiconductor for the design of its programmable logic. Based on VHDL, Warp3 uses graphics to ease design entry, timing verification and analysis, and waveform simulation. And because Warp3 is built on Viewlogic's CFI-compliant Powerview and Workview Plus frameworks, it provides an open environment that lets users migrate designs to ASICs, gate arrays, and to the board and system level. Warp3 supports Cypress' entire line of parts, including the UltraLogic family of FPGAs and complex PLDs. Users enter designs with a mixture of VHDL descriptions, Boolean expressions, state tables, and schematic diagrams. Regardless of the entry method, Warp3 translates the design into VHDL, compiles it, and synthesizes a logic-gate representation. It then fits the design into the chosen device, and generates a programming file. Warp3 runs on PCs under Windows, and on Sun workstations under OpenLook or Motif. Introductory pricing is set at \$4995 and \$7495, respectively. LM

Cypress Semiconductor Corp., 3901 N. First St., San Jose, CA 95134-1599; (408) 943-2600. **CIRCLE 120**

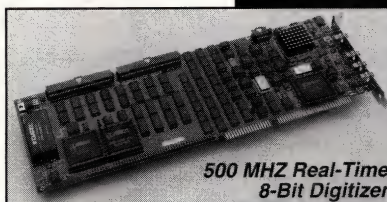
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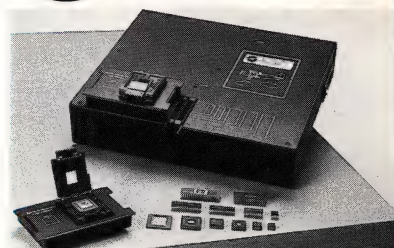
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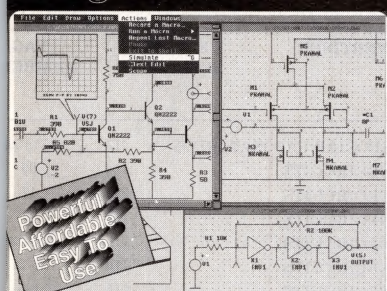
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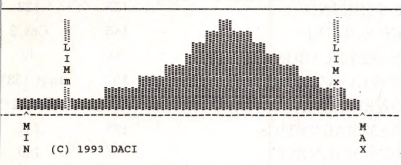
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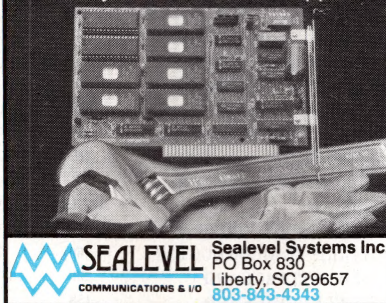
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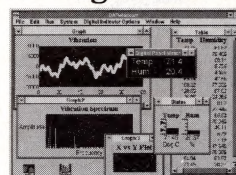
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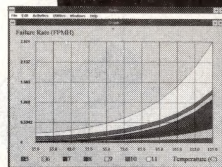
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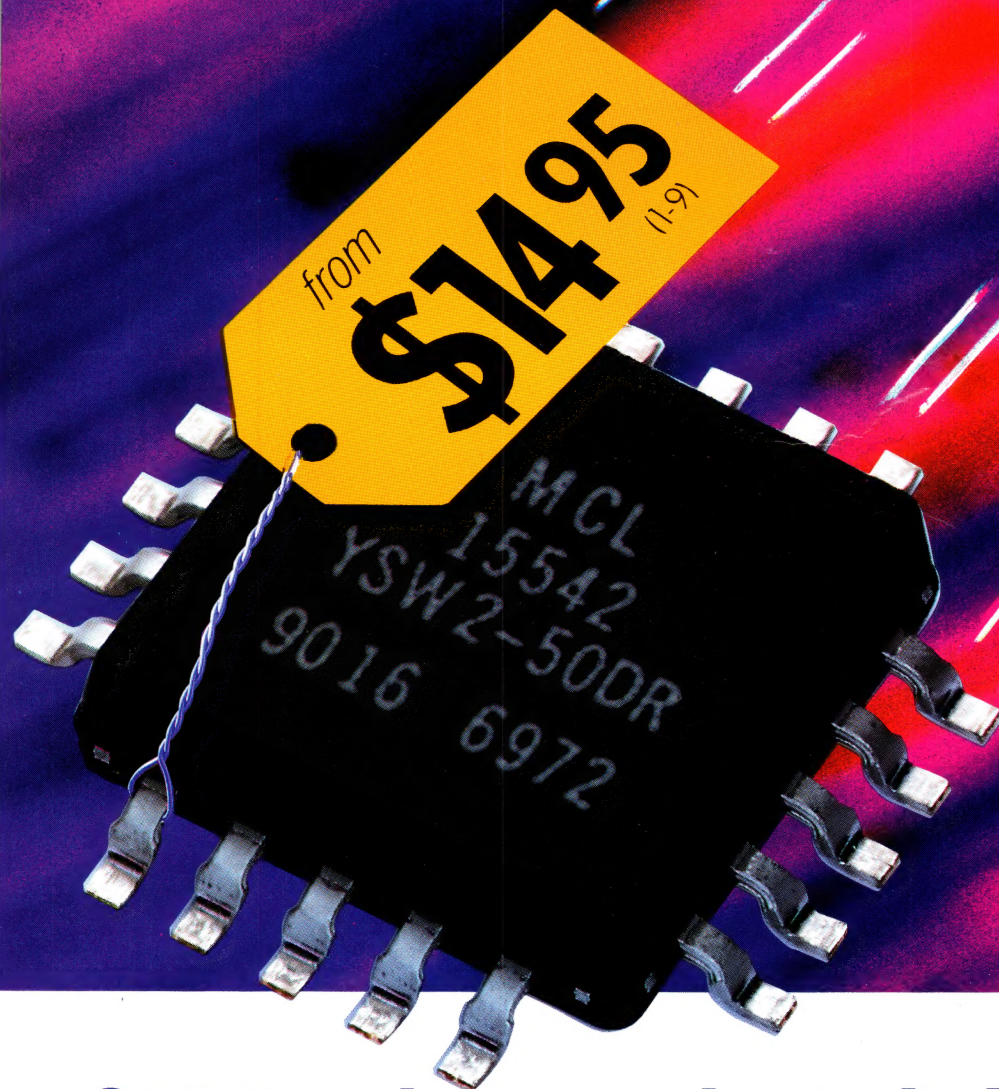
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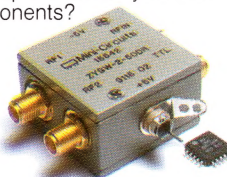


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Truly incredible...superfast 3nsec GaAs SPDT reflective or absorptive switches with built-in driver, available in pc plug-in or SMA connector models, from only \$14.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' latest innovative integrated components?

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SPECIFICATIONS (typ)

	Absorptive SPDT			Reflective SPDT		
	YSWA-2-50DR	ZYWSA-2-50DR		YSW-2-50DR	ZYWS-2-50DR	
Frequency (MHz)	dc- 500 2000 5000	500	2000	dc- 500 2000 5000	500	2000
Ins. Loss (dB)	1.1 1.4 1.9	1.1	1.4	0.9 1.3 1.4	0.9	1.3
Isolation (dB)	42 31 20	42	31	50 40 28	50	40
1dB Comp. (dBm)	18 20 22.5	18	20	20 20 24	20	20
RF Input (max dBm)	— 20 —	—	20	22 22 26	22	22
VSWR "on"	1.25 1.35 1.5	1.25	1.35	1.4 1.4 1.4	1.4	1.4
Video Bkthru (mV,p/p)	30 30 30	30	30	30 30 30	30	30
Sw. Spd. (nsec)	3 3 3	3	3	3 3 3	3	3
Price, \$	YSWA-2-50DR (pin) 23.95	YSWA-2-50DR (pin) 23.95		YSW-2-50DR (pin) \$14.95	YSW-2-50DR (pin) \$14.95	
(1-9 qty)	ZYWSA-2-50DR (SMA) 69.95	ZYWSA-2-50DR (SMA) 69.95		ZYWS-2-50DR (SMA) 59.95	ZYWS-2-50DR (SMA) 59.95	

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F141 REV. D

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3.3V and 5V High Efficiency Dual Step Down Switching Regulator.

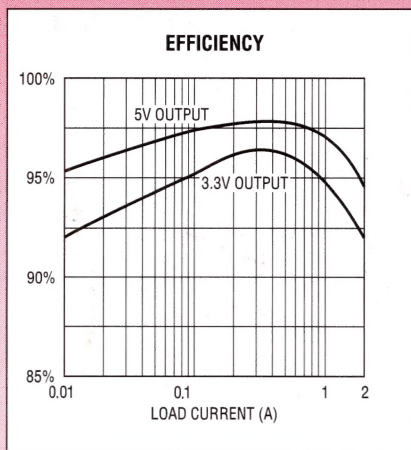
The LTC1142 dual-output ultra high-efficiency synchronous regulator controller, available in a compact 28-lead SSOP, maximizes battery life in a small amount of board space.



The LTC1143 dual-output high-efficiency regulator controller is available in a space-saving narrow 16-lead SOIC package.

Both devices feature advanced Burst Mode™ power management circuitry providing high efficiencies at load currents from a few milliamps to amps. Standby current is a low 160µA per regulator.

Both the LTC1142 and LTC1143 incorporate two independent regulator blocks providing 3.3V and 5V outputs with individual shutdown to less than 20µA. The LTC1142 operates over a 5V to 20V input range,



allowing 10-12 cell battery packs.

The LTC1142 also supports full synchronous MOSFET switching for both regulator sections for efficiencies which can exceed 95%. The LTC1143 uses the fewest external components in the least amount of board space with efficiencies around 90%.

These versatile controllers also provide short circuit protection, very low dropout operation and excellent transient response. Pricing starts at \$ 5.45 in 1000 piece quantities for the LTC1143CS.

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